SSC3S927

Description

The SSC3S927 is a controller with SMZ* method for LLC current resonant switching power supplies, incorporating a floating drive circuit for a high-side power MOSFET. The product includes useful functions such as Standby Function, Automatic Dead Time Adjustment, and Capacitive Mode Detection.

The product achieves high efficiency, low noise and high cost-effective power supply systems with few external components.

*SMZ: Soft-switched Multi-resonant Zero Current switch, achieved soft switching operation during all switching periods.

Package

SOP18

Not to scale

Features

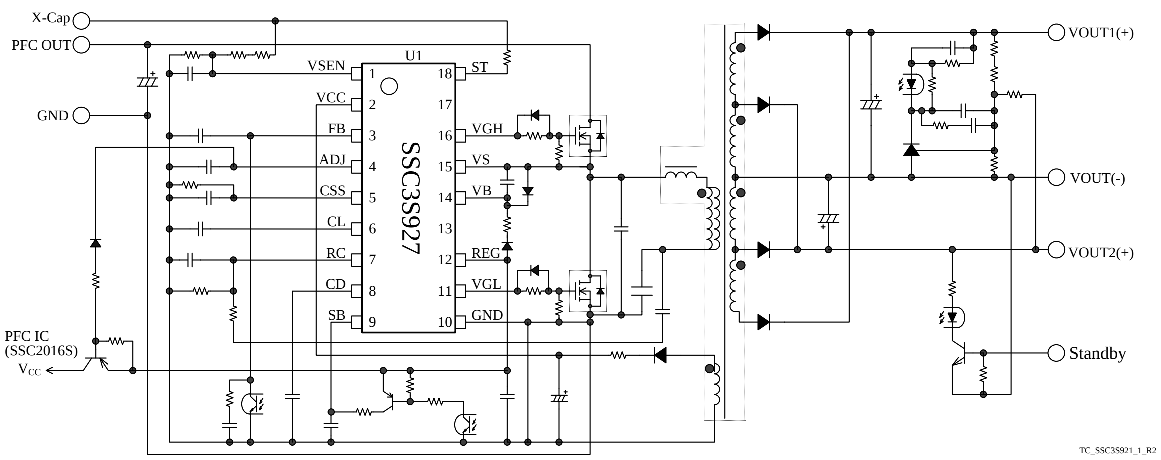
- Standby Mode Change Function
  - Output Power at Light Load: P_O = 150 mW (P_{IN} = 0.27 W)
  - Burst operation in standby mode
  - Soft-on/Soft-off function: reduces audible noise
- PFC IC ON/OFF Function: In standby operation, the IC turns off PFC IC.
- Soft-start Function
- Capacitive Mode Detection Function
- Reset Detection Function
- Automatic Dead Time Adjustment Function
- Brown-in and Brown-out Function
- X-capacitor Discharge Function
- Protections
  - High-side Driver UVLO: Auto-restart
  - Overcurrent Protection (OCP): Auto-restart, peak drain current detection, 2-step detection
  - Overload Protection (OLP): Auto-restart
  - Overvoltage Protection (OVP): Auto-restart
  - REG Overvoltage Protection (REG_OVP) : Auto-restart
  - Thermal Shutdown (TSD) : Auto-restart

Applications

Switching power supplies for electronic devices such as:

- Digital Appliances: LCD television and so forth
- Office Automation (OA) equipment: server, multi-function printer, and so forth
- Industrial Apparatus
- Communication Facilities

Typical Application



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Contents

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1. Absolute Maximum Ratings

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); and current coming out of the IC (sourcing) is negative current (−).

Unless otherwise specified, T_A is 25°C.

Characteristic	Symbol	Pins	Rating	Unit
VSEN Pin Sink Current	I_{SEN}	1 − 10	1.0	mA
Control Part Input Voltage	V_{CC}	2 − 10	−0.3 to 35	V
FB Pin Voltage	V_{FB}	3 − 10	−0.3 to 6	V
ADJ Pin Voltage	V_{ADJ}	4 − 10	−0.3 to V_{REG}	V
CSS Pin Voltage	V_{CSS}	5 − 10	−0.3 to 6	V
CL Pin Voltage	V_{CL}	6 − 10	−0.3 to 6	V
RC Pin Voltage	V_{RC}	7 − 10	−6 to 6	V
CD Pin Voltage	V_{CD}	8 − 10	−0.3 to 6	V
SB Pin Sink Current	I_{SB}	9 − 10	100	µA
VGL pin Voltage	V_{GL}	11 − 10	−0.3 to V_{REG} + 0.3	V
REG pin Source Current	I_{REG}	12 − 10	−10.0	mA
Voltage Between VB Pin and VS Pin	V_B−V_S	14 − 15	−0.3 to 20.0	V
VS Pin Voltage	V_S	15 − 10	−1 to 600	V
VGH Pin Voltage	V_{GH}	16 − 10	V_S − 0.3 to V_B + 0.3	V
ST Pin Voltage	V_{ST}	18 − 10	−0.3 to 600	V
Operating Ambient Temperature	T_{OP}	−	−40 to 85	°C
Storage Temperature	T_{stg}	−	−40 to 125	°C
Junction Temperature	T_j	−	150	°C

* Surge voltage withstand (Human body model) of No.14, 15 and 16 is guaranteed 1000V. Other pins are guaranteed 2000 V.

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2. Electrical Characteristics

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); and current coming out of the IC (sourcing) is negative current (−).

Unless otherwise specified, T_A is 25 °C, V_{CC} is 19 V.

Characteristic	Symbol	Conditions	Pins	Min.	Typ.	Max.	Unit
Start Circuit and Circuit Current							
Operation Start Voltage	$V_{CC(ON)}$		2 − 10	15.8	17.0	18.2	V
Operation Stop Voltage (1)	$V_{CC(OFF)}$		2 − 10	7.8	8.9	9.8	V
Startup Current Biasing Threshold Voltage(1)	$V_{CC(BIAS)}$		2 − 10	9.0	9.8	10.6	V
Circuit Current in Operation	$I_{CC(ON)}$		2 − 10	—	—	10.0	mA
Circuit Current in Non-Operation (2)	$I_{CC(OFF)}$	V_{CC} = 11 V	2 − 10	—	0.7	1.5	mA
Startup Current (2)	I_{ST}		18 − 10	3.0	6.0	9.0	mA
Protection Operation Release Threshold Voltage(1)	$V_{CC(P.OFF)}$		2 − 10	7.8	8.9	9.8	V
Circuit Current in Protection	$I_{CC(P)}$	V_{CC} = 10 V	2 − 10	—	0.7	1.5	mA
Oscillator							
Minimum Frequency	$f_{(MIN)}$		11 – 10 16 − 15	27.5	31.5	35.5	kHz
Maximum Frequency	$f_{(MAX)}$		11 – 10 16 − 15	230	300	380	kHz
Minimum Dead-Time	$t_{d(MIN)}$		11 – 10 16 − 15	0.04	0.24	0.44	μs
Maximum Dead-Time	$t_{d(MAX)}$		11 – 10 16 − 15	1.20	1.65	2.20	μs
Externally Adjusted Minimum Frequency 1	$f_{(MIN)ADJ1}$	R_{CSS} = 30 kΩ	11 – 10 16 − 15	69	73	77	kHz
Externally Adjusted Minimum Frequency 2	$f_{(MIN)ADJ2}$	R_{CSS} = 77 kΩ	11 – 10 16 − 15	42.4	45.4	48.4	kHz
Feedback Control							
FB Pin Oscillation Start Threshold Voltage	$V_{FB(ON)}$		3 – 10	0.15	0.30	0.45	V
FB Pin Oscillation Stop Threshold Voltage	$V_{FB(OFF)}$		3 – 10	0.05	0.20	0.35	V
FB Pin Maximum Source Current	$I_{FB(MAX)}$	V_{FB} = 0 V	3 – 10	−300	−195	−100	μA
FB Pin Reset Current	$I_{FB(R)}$		3 – 10	2.5	5.0	7.5	mA
Soft-start							
CSS Pin Charging Current	$I_{CSS(C)}$		5 – 10	−120	−105	−90	μA
CSS Pin Reset Current	$I_{CSS(R)}$	V_{CC} = 11V	5 – 10	1.1	1.8	2.5	mA
Maximum Frequency in Soft-start	$f_{(MAX)SS}$		11 – 10 16 − 15	400	500	600	kHz
Standby							
SB Pin Standby Threshold Voltage	$V_{SB(STB)}$		9 – 10	4.5	5.0	5.5	V
SB Pin Oscillation Start Threshold Voltage	$V_{SB(ON)}$		9 – 10	0.5	0.6	0.7	V

(1) $V_{CC(OFF)} = V_{CC(P.OFF)} < V_{CC(BIAS)}$ always.

(2) $I_{START} = I_{ST(OFF)} - I_{CC(OFF)}$,where, I_{START} is VCC pin sink current in startup.

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Characteristic	Symbol	Conditions	Pins	Min.	Typ.	Max.	Unit
SB Pin Oscillation Stop Threshold Voltage	$V_{SB(OFF)}$		9 – 10	0.4	0.5	0.6	V
SB Pin Clamp Voltage	$V_{SB(CLAMP)}$		9 – 10	7.0	8.5	10.0	V
SB Pin Source Current	$I_{SB(SRC)}$		9 – 10	−17	−10	−3	µA
SB Pin Sink Current	$I_{SB(SNK)}$		9 – 10	3	10	17	µA
CSS Pin Standby Release Threshold Voltage	$V_{CSS(STB)}$		5 – 10	1.35	1.50	1.65	V
PFC ON/OF Function							
ADJ Pin Voltage in Normal Operation	$V_{ADJ(L)}$		4 – 10	0	1	2	V
ADJ Pin Voltage in Standby Operation	$V_{ADJ(H)}$		4 – 10	8.5	9.9	10.8	V
ADJ Pin Threshold Voltage	V_{ADJ}		4 – 10	—	1.9	—	V
ADJ Pin Source Current	I_{ADJ}	V_{CC} = 11 V, V_{ADJ}= 0 V	4 – 10	−12.0	−10.2	−8.5	µA
Overload Protection (OLP)							
CL pin OLP Threshold Voltage	$V_{CL(OLP)}$		6 – 10	3.9	4.2	4.5	V
CL Pin Source Current 1	$I_{CL(SRC)1}$		6 – 10	−29	−17	−5	µA
CL Pin Source Current 2	$I_{CL(SRC)2}$		6 – 10	−180	−135	−90	µA
CL Pin Sink Current	$I_{CL(SNK)}$		6 – 10	10	30	50	µA
Brown-in and Brown-out							
VSEN Pin Threshold Voltage (On)	$V_{SEN(ON)}$		1 – 10	1.150	1.200	1.250	V
VSEN Pin Threshold Voltage (Off) 1	$V_{SEN(OFF)1}$		1 – 10	0.955	1.000	1.045	V
VSEN Pin Threshold Voltage (Off) 2	$V_{SEN(OFF)2}$		1 – 10	—	0.8	—	V
VSEN Pin HVP Threshold Voltage	$V_{SEN(HVP)}$		1 – 10	5.3	5.6	5.9	V
VSEN Pin Clamp Voltage	$V_{SEN\ (CLAMP)}$		1 – 10	10.0	—	—	V
VSEN pin Threshold Voltage for AC Line Detection 1	$V_{SEN(AC)1}$		1 – 10	2.56	2.70	2.84	V
VSEN Pin Threshold Voltage for AC Line Detection 2	$V_{SEN(AC)2}$		1 – 10	—	2.4	—	V
CD Pin Threshold Voltage 1	V_{CD1}		8 – 10	2.8	3.0	3.2	V
CD Pin Source Current	$I_{CD(SRC)}$	V_{CD} = 0 V	8 – 10	–12.0	–10.2	–8.5	µA
CD Pin Reset Current	$I_{CD(R)}$	V_{CD} = 2 V	8 – 10	1.0	2.5	4.0	mA
Reset Detection							
Maximum Reset Time	$t_{RST(MAX)}$		11 – 10 16 – 15	4	5	6	µs
Driver Circuit Power Supply							
VREG Pin Output Voltage	V_{REG}		12 – 10	9.6	10.0	10.8	V
High-side Driver							
High-side Driver Operation Start Voltage	$V_{BUV(ON)}$		14 – 15	5.7	6.8	7.9	V
High-side Driver Operation Stop Voltage	$V_{BUV(OFF)}$		14 – 15	5.5	6.4	7.3	V
Driver Circuit							

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Characteristic	Symbol	Conditions	Pins	Min.	Typ.	Max.	Unit
VGL,VGH Pin Source Current 1	$I_{GL(SRC)1}$ $I_{GH(SRC)1}$	V_{REG} = 10.5V V_B = 10.5V V_{GL} = 0V V_{GH} = 0V	11 – 10 16 – 15	—	–540	—	mA
VGL,VGH Pin Sink Current 1	$I_{GL(SNK)1}$ $I_{GH(SNK)1}$	V_{REG} = 10.5V V_B = 10.5V V_{GL} = 10.5V V_{GH} = 10.5V	11 – 10 16 – 15	—	1.50	—	A
VGL,VGH Pin Source Current 2	$I_{GL(SRC)2}$ $I_{GH(SRC)2}$	V_{REG} = 11.5V V_B = 11.5V V_{GL} = 10V V_{GH} = 10V	11 – 10 16 – 15	−140	−90	−40	mA
VGL,VGH Pin Sink Current 2	$I_{GL(SNK)2}$ $I_{GH(SNK)2}$	V_{REG} = 12V V_B = 12V V_{GL} = 1.5V V_{GH} = 1.5V	11 – 10 16 – 15	140	230	360	mA
Current Resonant and Overcurrent Protection(OCP)							
Capacitive Mode Detection Voltage 1	V_{RC1}		7 – 10	0.02	0.10	0.18	V
				−0.18	−0.10	−0.02	V
Capacitive Mode Detection Voltage 2	V_{RC2}		7 – 10	0.20	0.30	0.40	V
				−0.40	−0.30	−0.20	V
RC Pin Threshold Voltage (Low)	$V_{RC(L)}$		7 – 10	1.8	1.9	2.0	V
				−2.0	−1.9	−1.8	V
RC Pin Threshold Voltage (High speed)	$V_{RC(S)}$		7 – 10	2.62	2.80	2.98	V
				−2.98	−2.80	−2.62	V
CSS Pin Sink Current (Low)	$I_{CSS(L)}$		5 – 10	1.1	1.8	2.5	mA
CSS Pin Sink Current (High speed)	$I_{CSS(S)}$		5 – 10	13.0	20.5	28.0	mA
Overvoltage Protection (OVP)							
VCC Pin OVP Threshold Voltage	$V_{CC(OVP)}$		2 – 10	30.0	32.0	34.0	V
REG Pin OVP Threshold Voltage	$V_{CC(REG)}$		12 – 10	11.5	12.4	13.5	V
Thermal Shutdown (TSD)							
Thermal Shutdown Temperature	$T_{j(TSD)}$		—	140	—	—	°C
Thermal Resistance							
Junction to Ambient Thermal Resistance	$\theta_{j\text{-}A}$		—	—	—	95	°C/W

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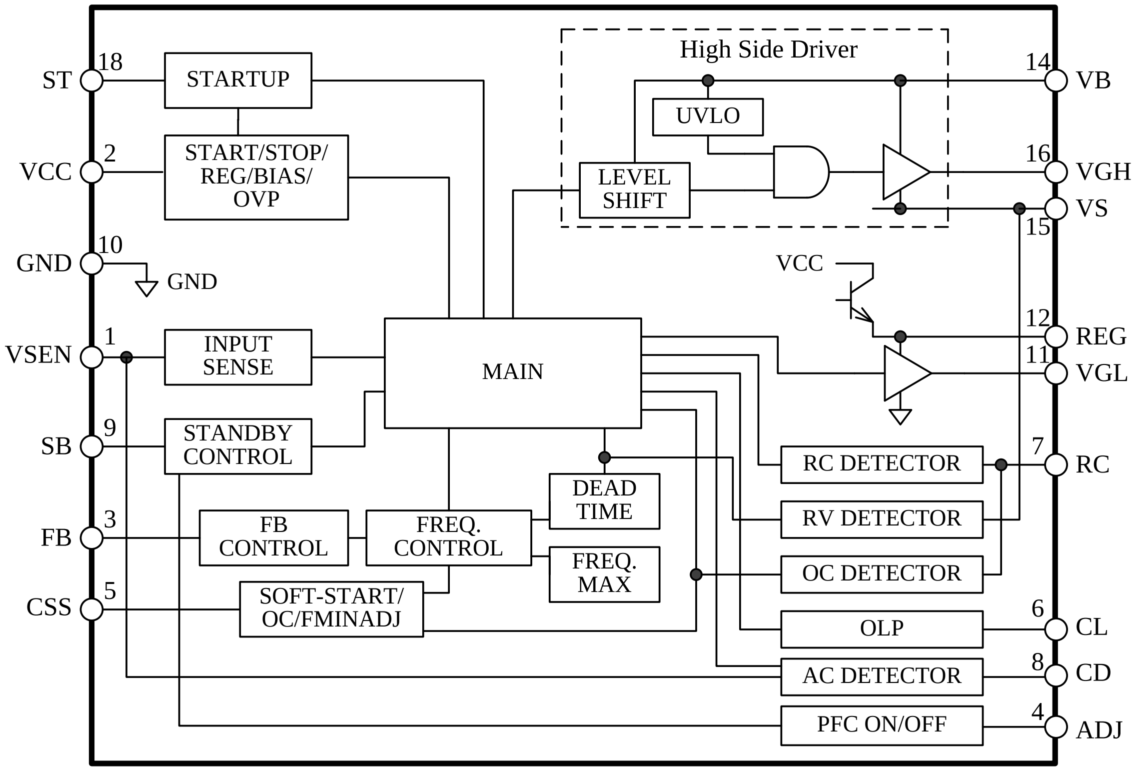
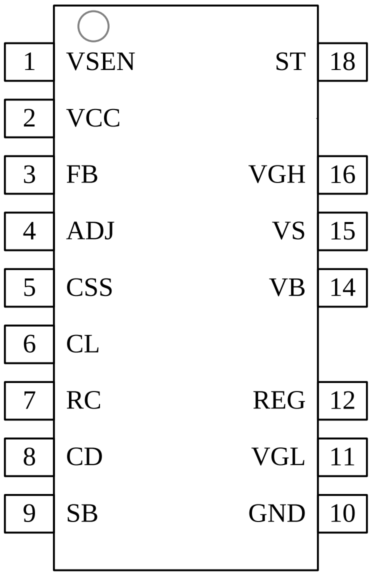
3. Block Diagram



BD_SSC3S927_R2

4. Pin Configuration Definitions



Number	Name	Function
1	VSEN	The mains input voltage detection signal input
2	VCC	Supply voltage input for the IC, and Overvoltage Protection (OVP) signal input
3	FB	Feedback signal input for constant voltage control
4	ADJ	PFC ON/OFF signal output
5	CSS	Soft-start capacitor connection
6	CL	Overload detection capacitor connection
7	RC	Resonant current detection signal input, and Overcurrent Protection (OCP) signal input
8	CD	Delay time setting capacitor connection
9	SB	Standby mode change signal input
10	GND	Ground
11	VGL	Low-side gate drive output
12	REG	Supply voltage output for gate drive circuit
13	—	(Pin removed)
14	VB	Supply voltage input for high-side driver
15	VS	Floating ground for high-side driver
16	VGH	High-side gate drive output
17	—	(Pin removed)
18	ST	Startup current input

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5. Typical Application

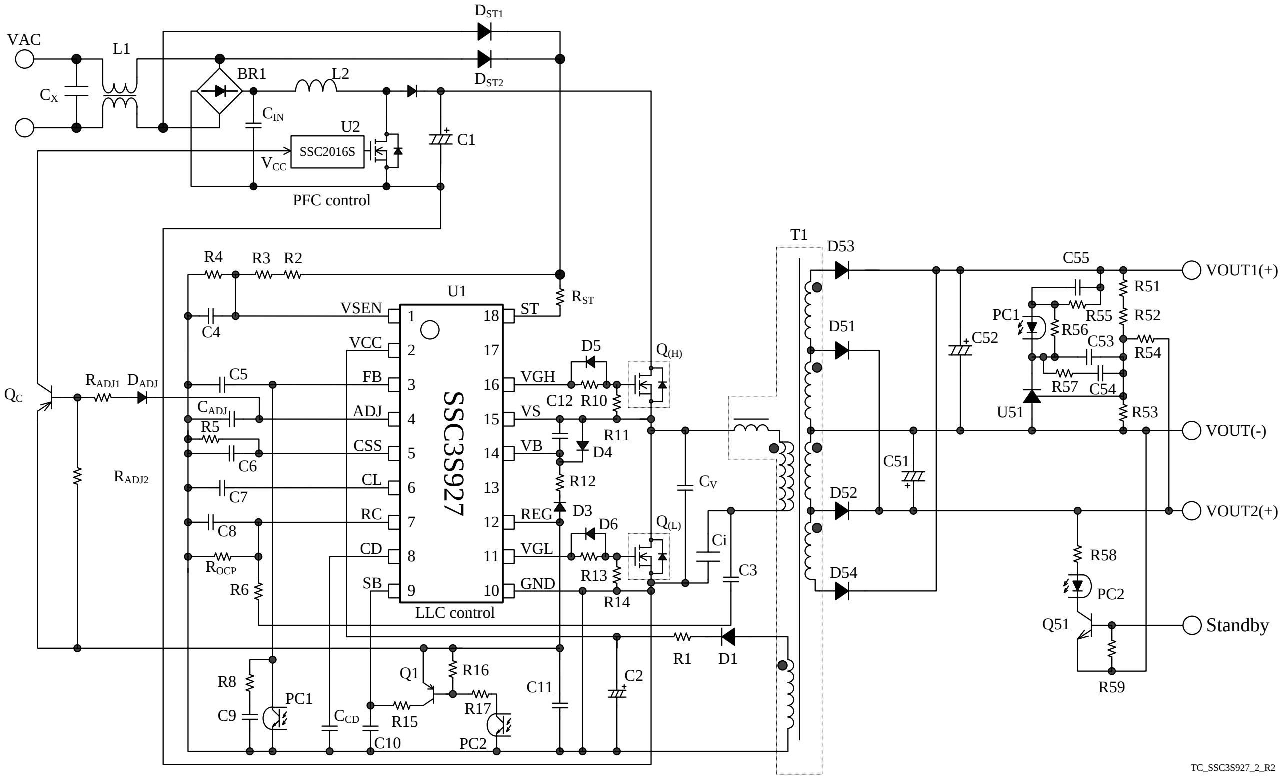

Figure 5-1. Typical Application

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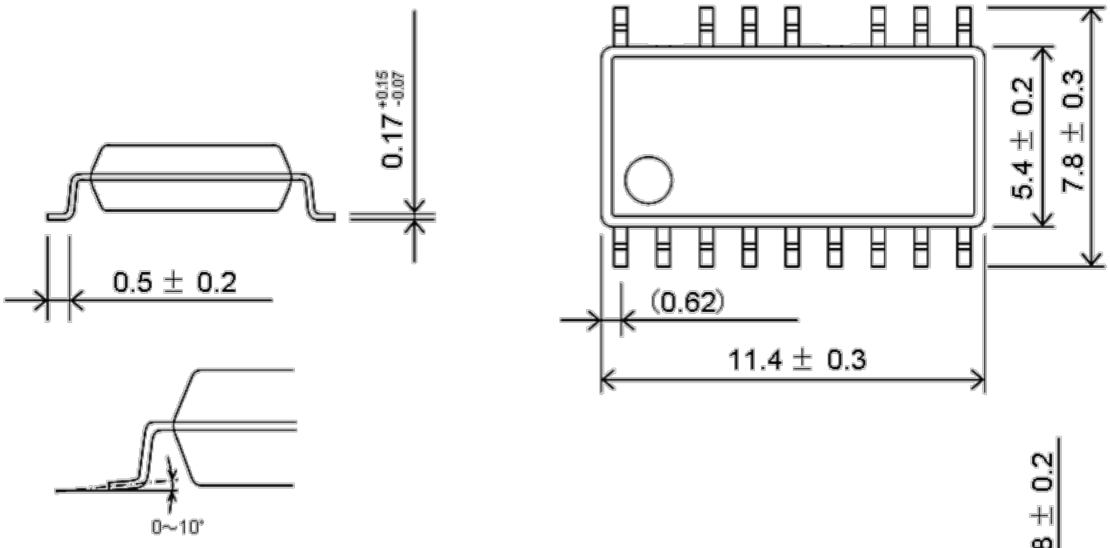
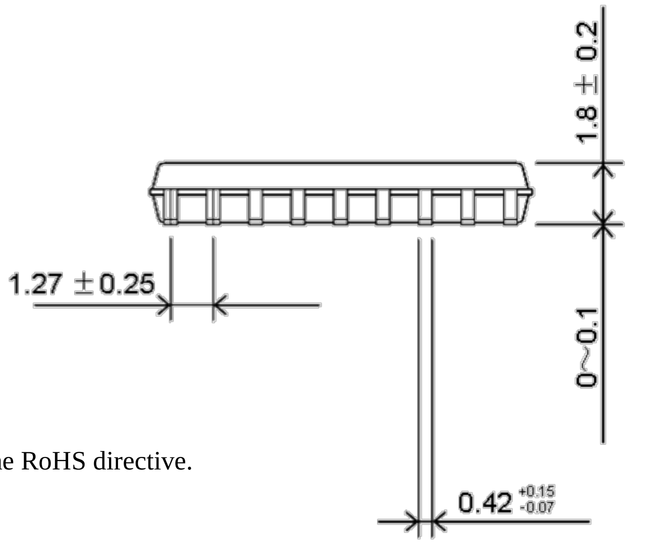
6. Physical Dimensions

- SOP18

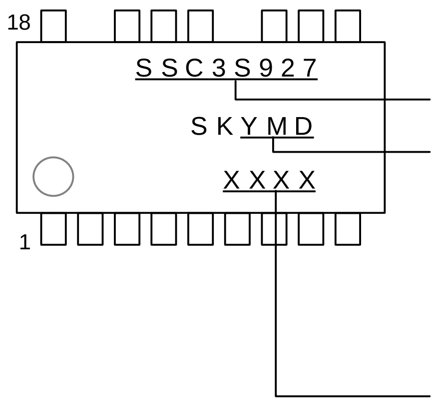




NOTES:

- Dimension is in millimeters.
- Pb-free. Device composition compliant with the RoHS directive.

7. Marking Diagram



Part Number

Lot Number:

Y is the last digit of the year of manufacture (0 to 9)

M is the month of the year (1 to 9, O, N, or D)

D is a period of days:

1: the first 10 days of the month (1st to 10th)

2: the second 10 days of the month (11th to 20th)

3: the last 10–11 days of the month (21st to 31st)

Control Number

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8. Operational Description

All of the parameter values used in these descriptions are typical values, unless they are specified as minimum or maximum.

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); and current coming out of the IC (sourcing) is negative current (−). $Q_{(H)}$ and $Q_{(L)}$ indicate a high-side power MOSFET and a low-side power MOSFET respectively. Ci, and C_V indicate a current resonant capacitor and a voltage resonant capacitor respectively.

8.1 Resonant Circuit Operation

Figure 8-1 shows a basic RLC series resonant circuit.

The impedance of the circuit, $\dot{Z}$, is as the following Equation.

$$\dot{Z} = R + j\left(\omega L - \frac{1}{\omega C}\right) \tag{1}$$

where, ω is angular frequency and ω = 2πf.

$$\dot{Z} = R + j\left(2\pi f L - \frac{1}{2\pi f C}\right) \tag{2}$$

When the frequency, f, changes, the impedance of resonant circuit will change as shown in Figure 8-2.

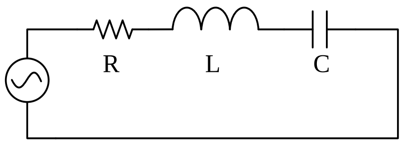

Figure 8-1. RLC Series Resonant Circuit

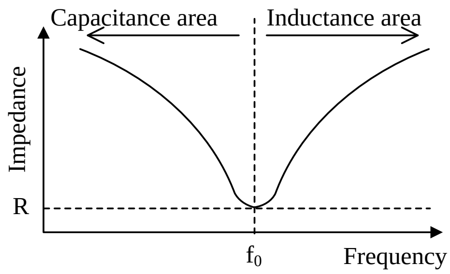

Figure 8-2. Impedance of Resonant Circuit

In Equation (2), $\dot{Z}$ becomes minimum value (= R) at 2πfL = 1/2πfC, and then ω is calculated by Equation (3) .

$$\omega = 2\pi f = \frac{1}{\sqrt{LC}} \tag{3}$$

The frequency in which $\dot{Z}$ becomes minimum value is the resonant frequency, f_0. The higher frequency area than f_0 is the inductance area, and the lower frequency area than f_0 is the capacitance area.

From Equation (3), f_0 is as follows;

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \tag{4}$$

Figure 8-3 shows the circuit of a current resonant power supply. The basic configuration of the current resonant power supply is a half-bridge converter. The switching device $Q_{(H)}$ and $Q_{(L)}$ are connected in series with V_{IN}. The series resonant circuit and the voltage resonant capacitor C_V are connected in parallel with $Q_{(L)}$. The series resonant circuit is comprised of a resonant inductor L_R, a primary winding P of a transformer T1 and a current resonant capacitor C_i. In the resonant transformer T1, the coupling between primary winding and secondary winding is designed to be poor so that the leakage inductance increases. By using it as L_R, the series resonant circuit can be down sized. The dotted mark in T1 shows the winding polarity, the secondary windings S1 and S2 are connected so that the polarities are set to the same position shown in Figure 8-3, and the winding numbers of each other are equal.

From Equation (1), the impedance of current resonant power supply is calculated by Equation (5). From Equation (4), the resonant frequency, f_0, is calculated by Equation (6).

$$\dot{Z} = R + j\left\{\omega(L_R + L_P) - \frac{1}{\omega Ci}\right\} \tag{5}$$

$$f_0 = \frac{1}{2\pi\sqrt{(L_R + L_P) \times Ci}} \tag{6}$$

where,
R is the equivalent resistance of load,
L_R is the inductance of the resonant inductor,
L_P is the inductance of the primary winding P, and
Ci is the capacitance of current resonant capacitor.

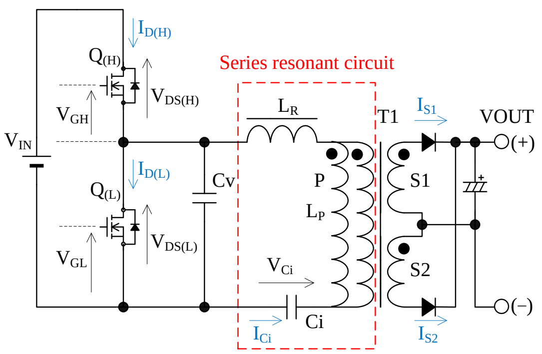

Figure 8-3. Current Resonant Power Supply Circuit

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In the current resonant power supply, $Q_{(H)}$ and $Q_{(L)}$ are alternatively turned on and off. The on time and off time of them are equal. There is a dead time between $Q_{(H)}$ on period and $Q_{(L)}$ on period. During the dead time, both $Q_{(H)}$ and $Q_{(L)}$ are in off status.

The current resonant power supply is controlled by the frequency control. When the output voltage decreases, the IC makes the switching frequency low so that the output power is increased and the output voltage is kept constant. This control must operate in the inductance area ($f_{SW} > f_0$). Since the winding current is delayed from the winding voltage in the inductance area, the turn-on operation is ZCS (Zero Current Switching) and the turn-off operation is ZVS (Zero Voltage Switching). Thus, the switching loss of $Q_{(H)}$ and $Q_{(L)}$ is nearly zero,

In the capacitance area ($f_{SW} < f_0$), the current resonant power supply operates as follows. When the output voltage decreases, the switching frequency is decreased, and then the output power is more decreased. Thus, the output voltage cannot be kept constant. Since the winding current goes ahead of the winding voltage in the capacitance area, the operation with hard switching occurs in $Q_{(H)}$ and $Q_{(L)}$. Thus, the power loss increases.

This operation in the capacitance area is called the capacitive mode operation. The current resonant power supply must be operated without the capacitive mode operation (see Section 8.11 about details of it).

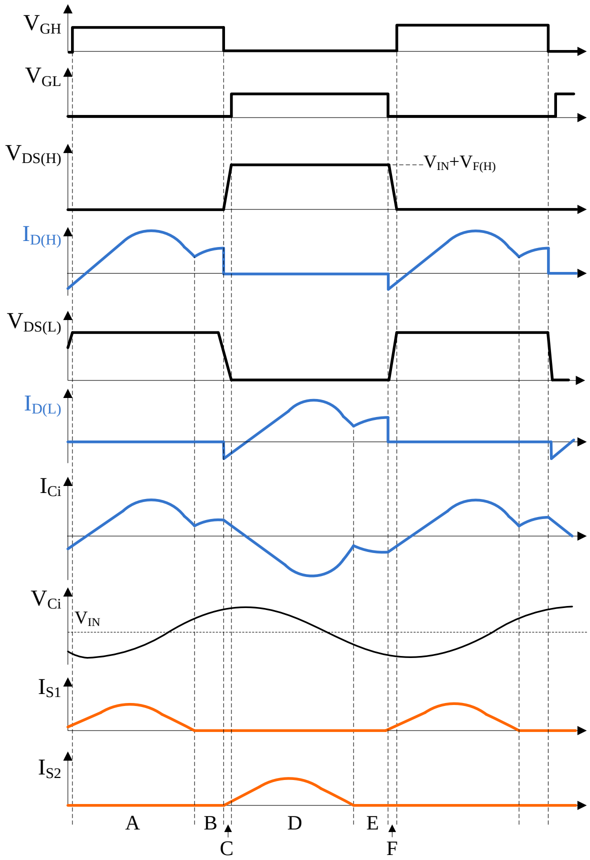

Figure 8-4. The Basic Operation Waveforms of Current Resonant Power Supply

Figure 8-4 shows the basic operation waveform of current resonant power supply (see Figure 8-3 about the symbol in Figure 8-4). The current resonant waveforms in normal operation are divided a period A to a period F. The current resonant power supply operates in the each period as follows.

In following description,
$I_{D(H)}$ is the current of $Q_{(H)}$,
$I_{D(L)}$ is the current of $Q_{(L)}$,
$V_{F(H)}$ is the forwerd voltage of $Q_{(H)}$,
$V_{F(L)}$ is the forwerd voltage of $Q_{(L)}$,
I_L is the current of L_R,
V_{IN} is an input voltage,
V_{Ci} is Ci voltage, and
V_{CV} is C_V voltage.

1) Period A

When $Q_{(H)}$ is ON, energy is stored into the series resonant circuit by $I_{D(H)}$ flowing through the resonant circuit and the transformer as shown in Figure 8-5. At the same time, the energy is transferred to the secondary circuit. When the primary winding voltage can not keep the secondary rectifier ON, the energy to the secondary circuit is stopped.

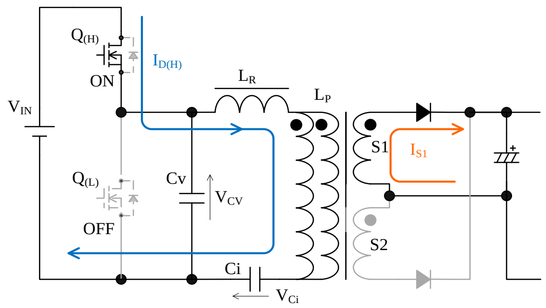

Figure 8-5. Operation in period A

2) Period B

After the secondary side current becomes zero, the resonant current flows to the primary side only as shown in Figure 8-6 and Ci is charged by it.

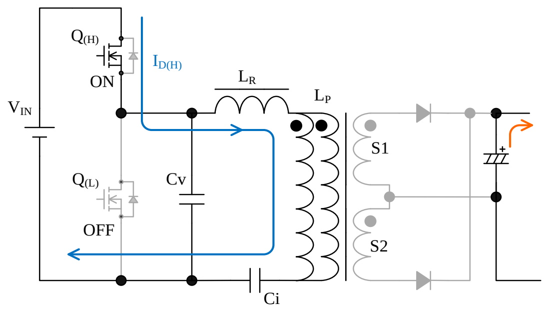

Figure 8-6. Operation in Period B

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3) Period C

Pireod C is the dead-time. Both $Q_{(H)}$ and $Q_{(L)}$ are in off-state.

When $Q_{(H)}$ turns off, I_L is flowed by the energy stored in the series resonant circuit as shown in Figure 8-7, and C_V is discharged. When V_{CV} decreases to $V_{F(L)}$, $-I_{D(L)}$ flows through the body diode of $Q_{(L)}$ and V_{CV} is clamped to $V_{F(L)}$.

After that, $Q_{(L)}$ turns on. Since $V_{DS(L)}$ is nearly zero at the point, $Q_{(L)}$ operates in ZVS and ZCS. Thus, switching loss is nearly zero.

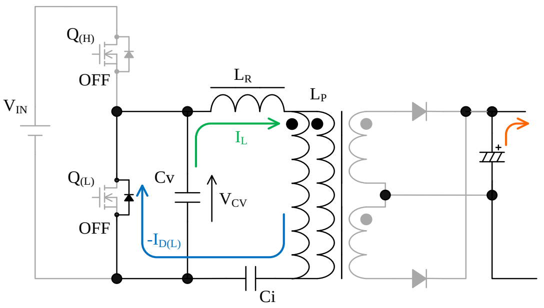

Figure 8-7. Operation in Period C

4) Period D

When $Q_{(L)}$ turns on, $I_{D(L)}$ flows as shown in Figure 8-8 and the primary winding voltage of the transformer adds V_{Ci}. At the same time, energy is transferred to the secondary circuit. When the primary winding voltage can not keep the secondary rectifier ON, the energy to the secondary circuit is stopped.

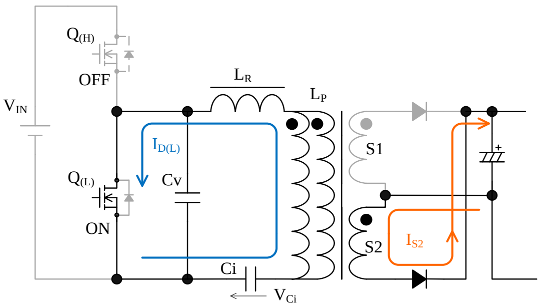

Figure 8-8. Operation in Period D

5) Period E

After the secondary side current becomes zero, the resonant current flows to the primary side only as shown in Figure 8-9 and Ci is charged by it.

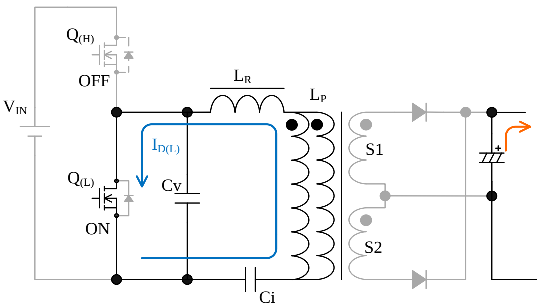

Figure 8-9. Operation in Period E

6) Period F

This pireod is the dead-time. Both $Q_{(H)}$ and $Q_{(L)}$ are in off-state.

When $Q_{(L)}$ turns off, $-I_L$ is flowed by the energy stored in the series resonant circuit as shown in Figure 8-10. C_V is discharged. When V_{CV} decreases to $V_{IN} + V_{F(H)}$, $-I_{D(H)}$ flows through body diode of $Q_{(H)}$ and V_{CV} is clamped to $V_{IN} + V_{F(H)}$.

After that, $Q_{(H)}$ turns on. Since $V_{DS(H)}$ is nearly zero at the point, $Q_{(H)}$ operates in ZVS and ZCS. Thus, the switching loss is nearly zero.

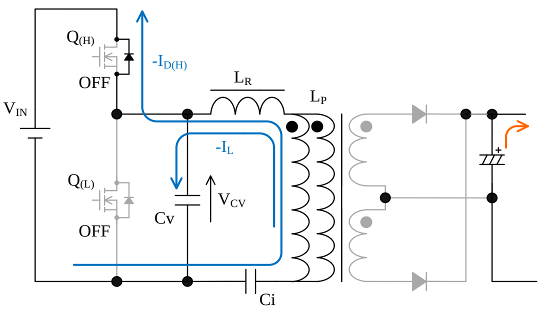

Figure 8-10. Operation in Period F

7) After the Period F

Then, $I_{D(H)}$ flows and the operation returns to the period A.

The above operation is repeated, the energy is transferred to the secondary side from the resonant circuit.

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8.2 Startup Operation

The IC has PFC IC ON/OFF Function.

Following subsections explain about the startup operation at PFC ON/OFF Function enable and disable.

8.2.1 PFC ON/OFF Function Enable

When PFC ON/OFF Function is enabled, the VCC pin should be set to $V_{CC(ON)}$ = 17.0 V after ADJ pin voltage reaches V_{ADJ} = 1.9 V or more at startup. Since source current I_{ADJ} = −10.2 µA flows from the ADJ pin, it is necessary to adjust the timing by the resistors and capacitors connected to the ADJ pin.

Figure 8-11 shows the VCC pin peripheral circuit. Figure 8-12 shows the startup operational waveforms.

The power supply starts as follows:

1) The mains input voltage is provided, and the VSEN pin voltage increases to the on-threshold voltage, $V_{SEN(ON)}$ = 1.200 V, or more.
2) The startup current, I_{ST}, which is a constant current of 6.0 mA is provided from the IC to capacitor C2 connected to the VCC pin, C2 is charged.
3) The ADJ pin voltage increases to V_{ADJ} = 1.9 V or more.
4) When the VCC pin voltage increases to the operation start voltage, $V_{CC(ON)}$ = 17.0 V, the control circuit of the IC is activated. After that, when the VSEN pin voltage reaches to $V_{SEN(ON)}$ = 1.200 V at the first-up edge of half-sinewave, REG pin voltage is output. At the same time, the ADJ pin outputs the PFC ON signal, and the PFC control IC is activated. The VCC pin voltage is decreased by the power dissipation of the IC.
5) When the VCC pin voltage decreases to $V_{CC(BIAS)}$ = 9.8 V, the C9 connected to FB pin starts to be charged. When the FB pin voltage increases to the oscillation start threshold voltage, $V_{FB(ON)}$ = 0.30 V, or more, the swiching operation starts.

After that, the startup circuit stops automatically, in order to eliminate its own power consumption.

During the IC operation, the rectified voltage from the auxiliary winding voltage, V_D, of Figure 8-11 is a power source to the VCC pin.

The winding turns of the winding D should be adjusted so that the VCC pin voltage is applied to equation (7) within the specification of the mains input voltage range and output load range of the power supply. The target voltage of the winding D is about 19 V.

$$V_{CC(BIAS)} < V_{CC} < V_{CC(OVP)}$$

$$\Rightarrow 9.8\ (V) < V_{CC} < 32.0\ (V) \qquad (7)$$

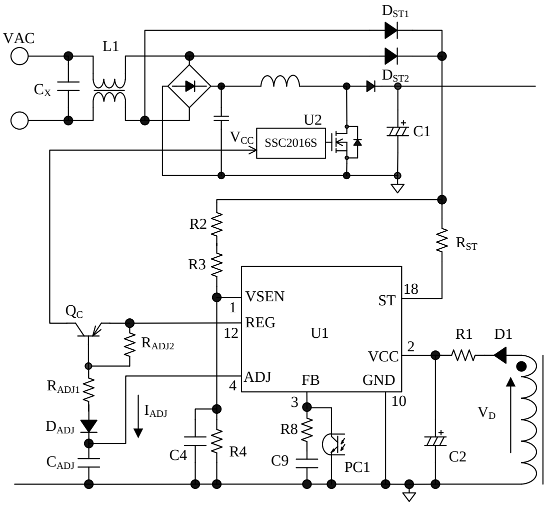

Figure 8-11. VCC Pin Peripheral Circuit When PFC ON/OFF Function is Enabled

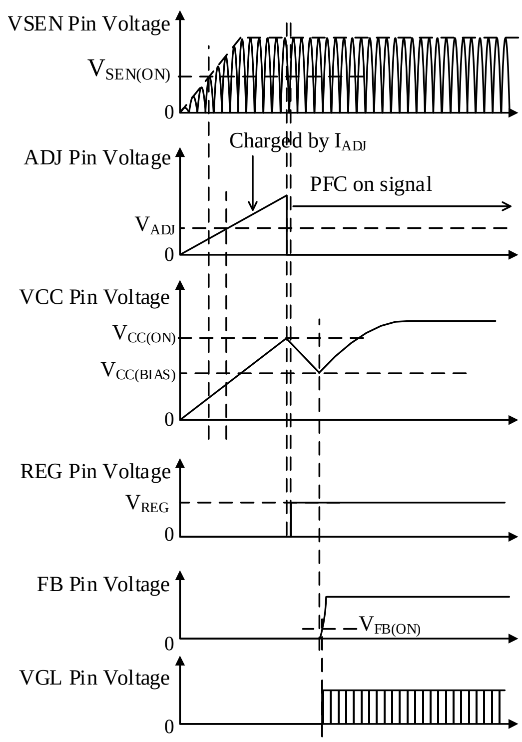

Figure 8-12. Startup Operation When PFC ON/OFF Function is Enabled

8.2.2 PFC ON/OFF Function Disable

When PFC ON/OFF Function is disabled, the pull-down resistor should be connected between ADJ pin and GND pin as shown in Figure 8-13. The pull-down resistors R_{ADJ} is recommended to 100 kΩ or less. The waveform at startup is shown in Figure 8-14.

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1) The mains input voltage is provided, and the VSEN pin voltage increases to the on-threshold voltage, $V_{SEN(ON)}$ = 1.200 V, or more.
2) The startup current, I_{ST}, which is a constant current of 6.0 mA is provided from the IC to capacitor C2 connected to the VCC pin, C2 is charged. When the VCC pin voltage increases to the operation start voltage, $V_{CC(ON)}$ = 17.0 V, the control circuit of the IC is activated. After that, when the VSEN pin voltage reaches to $V_{SEN(ON)}$ = 1.200 V at the first-up edge of half-sinewave, REG pin voltage is output.
3) The capacitor C9 connected to FB pin starts to be charged. When the FB pin voltage increases to the oscillation start threshold voltage, $V_{FB(ON)}$ = 0.30 V, or more, the swiching operation starts.

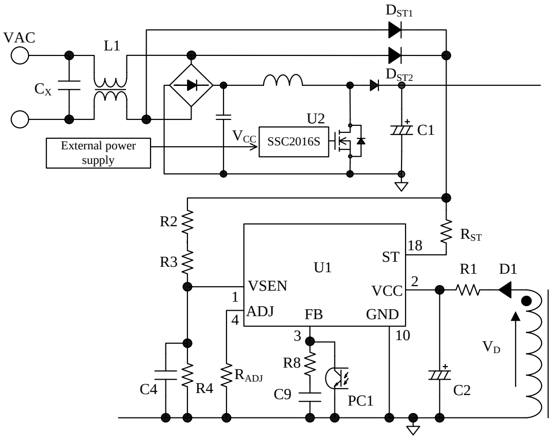

Figure 8-13. VCC Pin Peripheral Circuit When PFC ON/OFF Function is Disabled

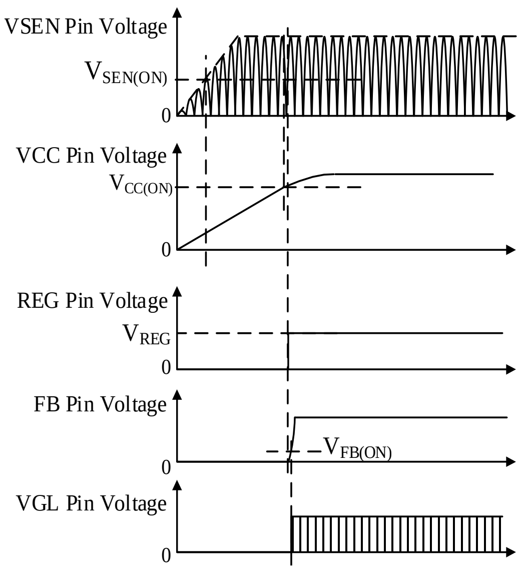

Figure 8-14. The Startup Operation When PFC ON/OFF Function Disabled

8.3 Undervoltage Lockout (UVLO)

Figure 8-15 shows the relationship of V_{CC} and I_{CC}.

After the IC starts operation, when the VCC pin voltage decreases to $V_{CC(OFF)}$ = 8.9 V, the IC stops switching operation by the Undervoltage Lockout (UVLO) Function and reverts to the state before startup again.

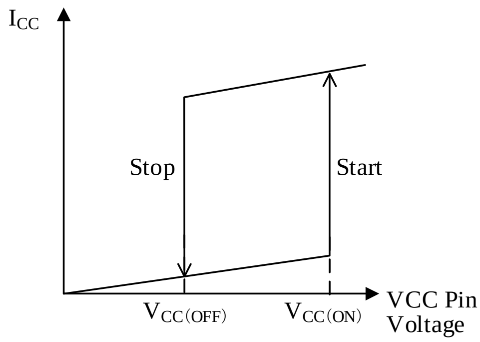

Figure 8-15. V_{CC} vs. I_{CC}

8.4 Bias Assist Function

Figure 8-16 shows the VCC pin voltage behavior during the startup period.

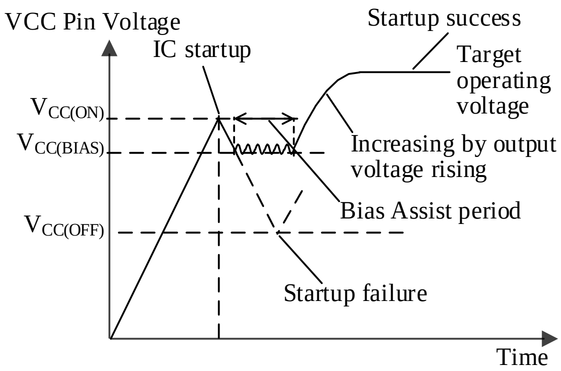

Figure 8-16. VCC Pin Voltage during Startup Period

When the conditions of Section 8.2 are fulfilled, the IC starts operation. Thus, the circuit current, I_{CC}, increases, and the VCC pin voltage begins dropping. At the same time, the auxiliary winding voltage, V_D, increases in proportion to the output voltage rise. Thus, the VCC pin voltage is set by the balance between dropping due to the increase of I_{CC} and rising due to the increase of the auxiliary winding voltage, V_D.

When the VCC pin voltage decreases to $V_{CC(OFF)}$ = 8.9 V, the IC stops switching operation and a startup failure occurs.

In order to prevent this, when the VCC pin voltage decreases to the startup current threshold biasing voltage, $V_{CC(BIAS)}$ = 9.8 V, the Bias Assist Function is activated.

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While the Bias Assist Function is activated, any decrease of the VCC pin voltage is counteracted by providing the startup current, I_{ST}, from the startup circuit.

It is necessary to check the startup process based on actual operation in the application, and adjust the VCC pin voltage, so that the startup failure does not occur.

If VCC pin voltage decreases to $V_{CC(BIAS)}$ and the Bias Assist Function is activated, the power loss increases.

Thus, VCC pin voltage in operation should be set more than $V_{CC(BIAS)}$ by the following adjustments.

- The turns ratio of the auxiliary winding to the secondary-side winding is increased.
- The value of C2 in Figure 8-11 is increased and/or the value of R1 is reduced.

During all protection operation, the Bias Assist Function is disabled.

8.5 Soft Start Function

Figure 8-17 shows the Soft-start operation waveforms.

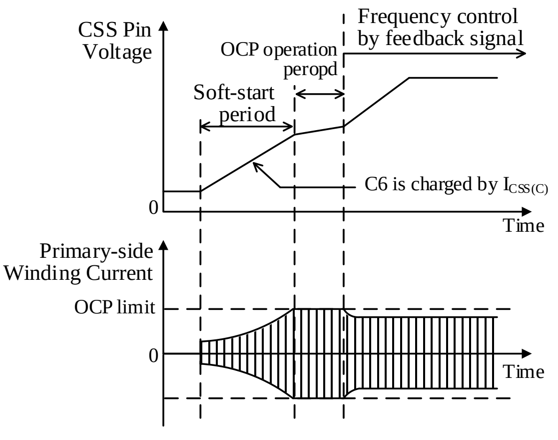

Figure 8-17. Soft-start Operation

The IC has Soft Start Function to reduce stress of peripheral component and prevent the capacitive mode operation.

During the soft start operation, C6 connected to the CSS pin is charged by the CSS Pin Charge Current, $I_{CSS(C)} = -105$ μA. The oscillation frequency is varied by the CSS pin voltage. The switching frequency gradually decreases from $f_{(MAX)SS}$* = 500 kHz at most, according to the CSS pin voltage rise. At same time, output power increases. When the output voltage increases, the IC is operated with an oscillation frequency controlled by feedback.

* The maximum frequency during normal operation is $f_{(MAX)} = 300$ kHz.

When the IC becomes any of the following conditions, C6 is discharged by the CSS Pin Reset Current, $I_{CSS(R)} = 1.8$ mA.

- The VCC pin voltage decreases to the operation stop voltage, $V_{CC(OFF)} = 8.9$ V, or less.
- After AC input voltage turns off, thr CD pin voltage increases to $V_{CD1} = 3.0$ V or more.
- Any of protection operations in protection mode (OVP, HVP, OLP or TSD) is activated.

8.6 Minimum and Maximum Switching Frequency Setting

The minimum switching frequency is adjustable by the value of R5 (R_{CSS}) connected to the CSS pin. The relationship of R5 (R_{CSS}) and the externally adjusted minimum frequency, $f_{(MIN)ADJ}$, is shown in Figure 8-18.

The $f_{(MIN)ADJ}$ should be adjusted to more than the resonant frequency, f_O, under the condition of the minimum mains input voltage and the maximum output power. The maximum switching frequency, f_{MAX}, is determined by the inductance and the capacitance of the resonant circuit. The f_{MAX} should be adjusted to less than the maximum frequency, $f_{(MAX)} = 300$ kHz.

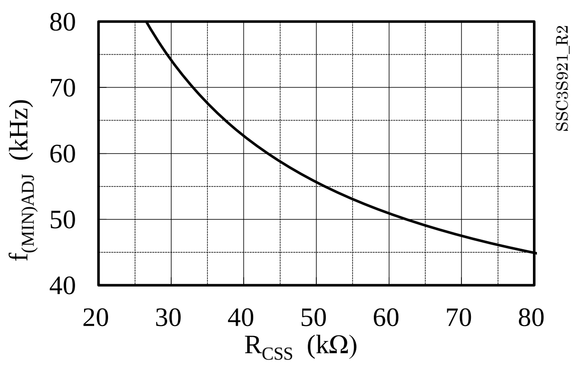

Figure 8-18. R5 (R_{CSS}) vs. $f_{(MIN)ADJ}$

8.7 High-side Driver

Figure 8-19 shows a bootstrap circuit. The bootstrap circuit is for driving to $Q_{(H)}$ and is made by D3, R12 and C12 between the REG pin and the VS pin.

When $Q_{(H)}$ is OFF state and $Q_{(L)}$ is ON state, the VS pin voltage becomes about ground level and C12 is charged from the REG pin.

When the voltage of between the VB pin and the VS pin, V_{B-S}, increases to $V_{BUV(ON)} = 6.8$ V or more, an internal high-side drive circuit starts operation. When V_{B-S} decreases to $V_{BUV(OFF)} = 6.4$ V or less, its drive circuit stops operation. In case the both ends of C12 and D4 are short, the IC is protected by $V_{BUV(OFF)}$. D4 for protection against negative voltage of the VS pin

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- D3
  D3 should be an ultrafast recovery diode of short recovery time and low reverse current. As for Sanken's diode lineup, AG01A (V_{RM} = 600 V) of UFRD series is recommended for the specification that the maximum mains input voltage is 265VAC.

- C11, C12, and R12
  The values of C11, C12, and R12 are determined by total gate charge, Qg, of external MOSFET and voltage dip amount between the VB pin and the VS pin in the burst mode of the standby mode change.
  C11, C12, and R12 should be adjusted so that the voltage between the VB pin and the VS is more than $V_{BUV(ON)}$ = 6.8 V by measuring the voltage with a high-voltage differential probe.
  The reference value of C11 is 0.47µF to 1 µF.
  The time constant of C12 and R12 should be less than 500 ns. The values of C12 and R22 are 0.047µF to 0.1 µF, and 2.2 Ω to 10 Ω.
  C11 and C12 should be a film type or ceramic capacitor of low ESR and low leakage current.

- D4
  D4 should be a Schottky diode of low forward voltage, V_F, so that the voltage between the VB pin and the VS pin must not decrease to the absolute maximum ratings of −0.3 V or less.

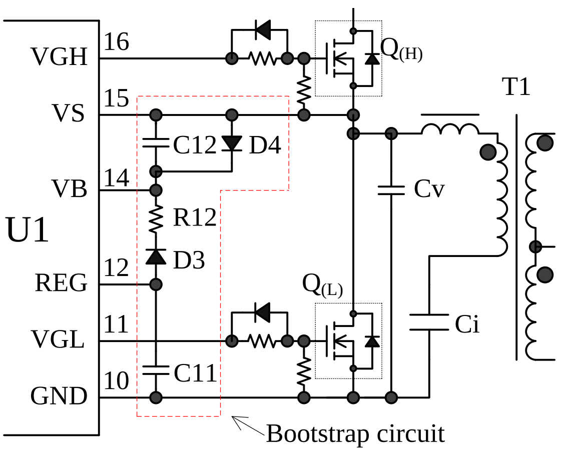

Figure 8-19. Bootstrap Circuit

8.8 Constant Voltage Control Operation

Figure 8-20 shows the FB pin peripheral circuit. The FB pin is sunk the feedback current by the photo-coupler, PC1, connected to FB pin. As a result, since the oscillation frequency is controlled by the FB pin, the output voltage is controlled to constant voltage (in inductance area).

The feedback current increases under slight load condition, and thus the FB pin voltage decreases. While the FB pin voltage decreases to the oscillation stop threshold voltage, $V_{FB(OFF)}$ = 0.20 V, or less, the IC stops switching operation. This operation reduces switching loss, and prevents the increasing of the secondary output voltage. In Figure 8-20, R8 and C9 are for phase compensation adjustment, and C5 is for high frequency noise rejection.

The secondary-side circuit should be designed so that the collector current of PC1 is more than 195 µA which is the absolute value of the maximum source current, $I_{FB(MAX)}$. Especially the current transfer ratio, CTR, of the photo coupler should be taken aging degradation into consideration.

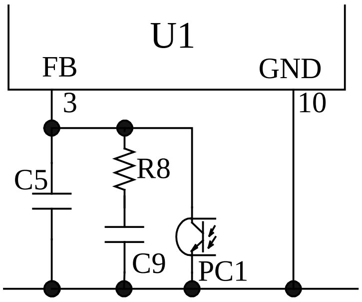

Figure 8-20. FB Pin Peripheral Circuit

8.9 Standby Function

The IC has the Standby Function in order to increase circuit efficiency in light load. When the Standby Function is activated, the IC operates in the burst oscillation mode as shown in Figure 8-21.

The burst oscillation has periodic non-switching intervals. Thus, the burst mode reduces switching losses. Generally, to improve efficiency under light load conditions, the frequency of the burst mode becomes just a few kilohertz. In addition, the IC has the Soft-on and the Soft-off Function in order to suppress rapid and sharp fluctuation of the drain current during the burst mode. thus, the audible noises can be reduced (see Section 8.9.2). The operation of the IC changes to the standby operation by the external signal (see Section 8.9.1).

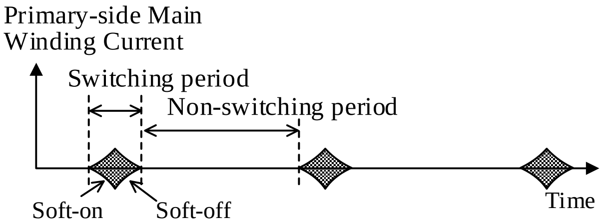

Figure 8-21. Standby Waveform

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8.9.1 Standby Mode Changed by External Signal

Figure 8-22 shows the standby mode change circuit with external signal. Figure 8-23 shows the standby change operation waveforms.
When the standby terminal of Figure 8-22 is provided with the L signal, Q1 turns off, C10 connected to the SB pin is discharged by the sink current, $I_{SB(SNK)}$ = 10 µA, and the SB pin voltage decreases. When the SB pin voltage decrease to the SB Pin Oscillation Stop Threshold Voltage, $V_{SB(OFF)}$ = 0.5 V, the operation of the IC is changed to the standby mode. When SB pin voltage is $V_{SB(OFF)}$ = 0.5 V or less and FB pin voltage is Oscillation Stop Threshold Voltage $V_{FB(OFF)}$ = 0.20 V or less, the IC stops switching operation. When the standby terminal is provided with the H signal and the SB pin voltage increases to Standby Threshold Voltage $V_{SB(STB)}$ = 5.0 V or more, the IC returns to normal operation.

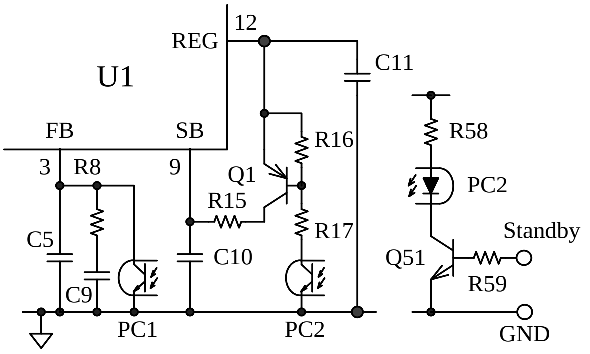

Figure 8-22. Standby Mode Change Circuit

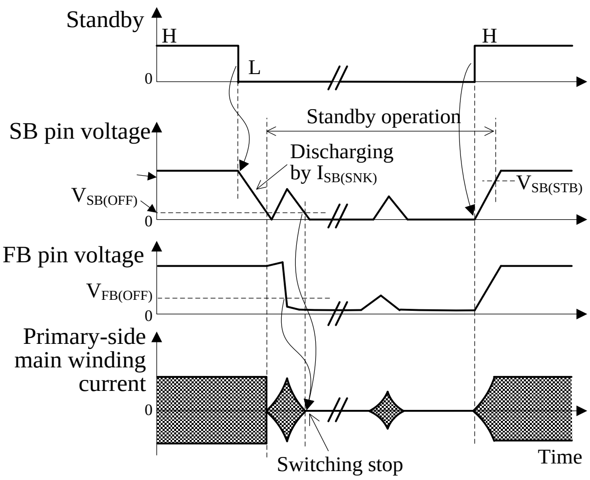

Figure 8-23. Standby Change Operation Waveforms

8.9.2 Burst Oscillation Operation

In standby operation, the IC operates burst oscillation where the peak drain current is suppressed by Soft-On /Soft-off Function in order to reduce audible noise from transformer. During burst oscillation operation, the switching oscillation is controlled by SB pin voltage.

Figure 8-24 shows the burst oscillation operation waveforms.

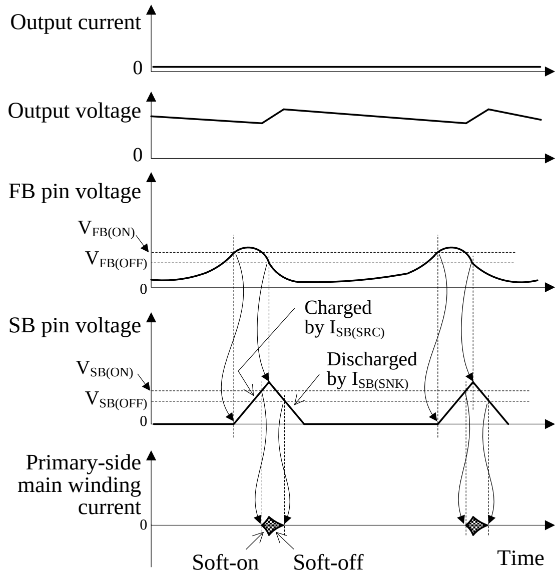

Figure 8-24. Burst Oscillation Operation Waveforms

When the SB pin voltage decreases to $V_{SB(OFF)}$ = 0.5 V or less and the FB pin voltage decreases to $V_{FB(OFF)}$ = 0.20 V or less, the IC stops switching operation and the output voltage decreases. Since the output voltage decreases, the FB pin voltage increases. When the FB pin voltage increases to the oscillation start threshold voltage, $V_{FB(ON)}$ = 0.30 V, C10 is charged by $I_{SB(SRC)}$ = −10 µA, and the SB pin voltage gradually increases. When the SB pin voltage increases to the oscillation start threshold voltage, $V_{SB(ON)}$ = 0.6 V, the IC resumes switching operation, controlling the frequency control by the SB pin voltage. Thus, the output voltage increases (Soft-on). After that, when FB pin voltage decrease to oscillation stop threshold voltage, $V_{FB(OFF)}$ = 0.20 V, C10 is discharged by $I_{SB(SNK)}$ = 10 µA and SB pin voltage decreases. When the SB pin voltage decreases to $V_{SB(OFF)}$ again, the IC stops switching operation. Thus, the output voltage decreases (Soft-off).

The SB pin discharge time in the Soft-on and Soft-off Function depends on C10. When the value of C10 increases, the Soft-On/Soft-off Function makes the peak drain current suppressed, and makes the burst period longer. Thus, the output ripple voltage may increase and/or the VCC pin voltage may decrease. If the VCC pin voltage decreases to $V_{CC(BIAS)}$ = 9.8 V, the Bias

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Assist Function is always activated, and it results in the increase of power loss (see Section 8.4).

Thus, it is necessary to adjust the value of C10 while checking the input power, the output ripple voltage, and the VCC pin voltage. The reference value of C10 is about 0.001 µF to 0.1 µF.

8.9.3 PFC ON/OFF Function

Figure 8-25 shows the operational waveform of PFC ON/OFF Output Function. When output power decreases and SB pin voltage reaches to $V_{SB(OFF)}$ = 0.5 V, the PFC ON/OFF Function activates and ADJ pin voltage increases to ADJ Pin Voltage in Standby Operation, $V_{ADJ(H)} = V_{REG}$ = 10.0 V. When output power increases and SB pin voltage reaches to $V_{SB(STB)}$ = 5.0 V, the ADJ pin voltage decreases to ADJ Pin Voltage in Normal Operation, $V_{ADJ(L)}$ = 1 V.

Using the signal, the power supply of PFC control IC can be turned on/off when the IC becomes standby operation. When the operation starting voltage of PFC IC, $V_{CC(ON)\_PFC}$, is less than V_{REG}, the PFC circuit on/off system can be realized by low component count as shown in Figure 8-26. SSC2016S that is Sanken PFC control IC is recommended.

When not using PFC ON/OFF signal, the pull-down resistor should be connected between ADJ pin and GND pin. (ADJ pin before the activation is set to less than V_{ADJ} = 1.9 V)

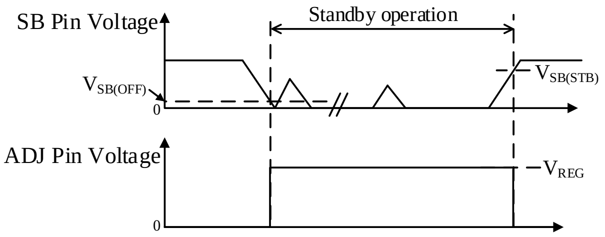

Figure 8-25. PFC ON/OFF Function

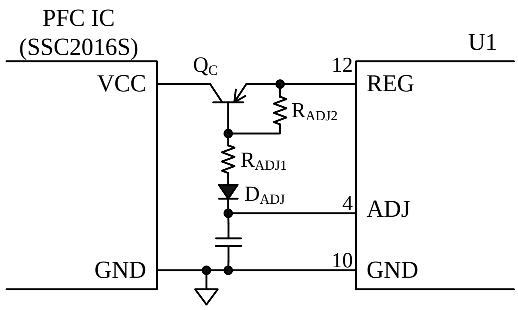

Figure 8-26. Typical Circuit That PFC IC is Stopped by the ADJ Pin Signal ($V_{CC(ON)\_PFC} < V_{REG}$)

8.10 Automatic Dead Time Adjustment Function

The dead time is the period when both the high-side and the low-side power MOSFETs are off.

As shown in Figure 8-27, if the dead time is shorter than the voltage resonant period, the power MOSFET is turned on and off during the voltage resonant operation. In this case, the power MOSFET turned on and off in hard switching operation, and the switching loss increases. The Automatic Dead Time Adjustment Function is the function that the ZVS (Zero Voltage Switching) operation of $Q_{(H)}$ and $Q_{(L)}$ is controlled automatically by the voltage resonant period detection of IC. The voltage resonant period is varied by the power supply specifications (input voltage and output power, etc.). However, the power supply with this function is unnecessary to adjust the dead time for each power supply specification.

As shown in Figure 8-28, the VS pin detects the dv/dt period of rising and falling of the voltage between drain and source of the low-side power MOSFET, $V_{DS(L)}$, and the IC sets its dead time to that period. This function controls so that the high-side and the low-side power MOSFETs are automatically switched to Zero Voltage Switching (ZVS) operation. This function operates in the period from $t_{d(MIN)}$ = 0.24 µs to $t_{d(MAX)}$ = 1.65 µs.

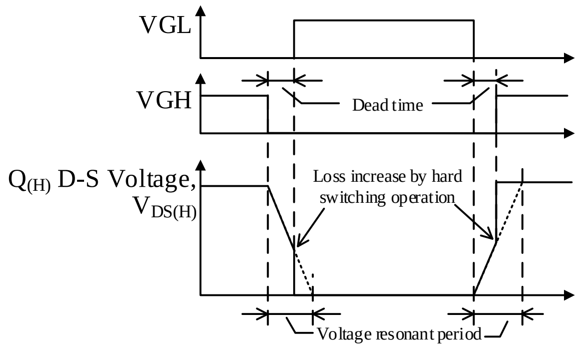

Figure 8-27. ZVS Failure Operation Waveform

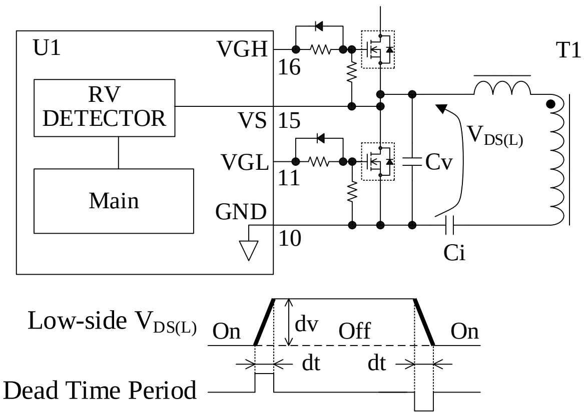

Figure 8-28. VS Pin and Dead Time Period

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In minimum output power at maximum input voltage and maximum output power at minimum input voltage, the ZCS (Zero Current Switching) operation of IC (the drain current flows through the body diode is about 600 ns as shown in Figure 8-29), should be checked based on actual operation in the application.

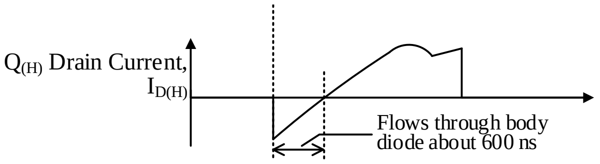

Figure 8-29. ZCS Check Point

8.11 Capacitive Mode Detection Function

The resonant power supply is operated in the inductance area shown in Figure 8-30. In the capacitance area, the power supply becomes the capacitive mode operation (see Section 8.1). In order to prevent the operation, the minimum oscillation frequency is needed to be set higher than f_0 on each power supply specification. However, the IC has the capacitive mode operation Detection Function kept the frequency higher than f_0. Thus, the minimum oscillation frequency setting is unnecessary and the power supply design is easier. In addition, the ability of transformer is improved because the operating frequency can operate close to the resonant frequency, f_0.

The resonant current is detected by the RC pin, and the IC prevents the capacitive mode operation. When the capacitive mode is detected, the C7 connected to CL pin is charged by $I_{CL(SRC)1}$ = −17 µA. When the CL pin voltage increases to $V_{CL(OLP)}$, the OLP is activated and the switching operation stops. During the OLP operation, the intermittent operation by UVLO is repeated (see Section 8.18). The detection voltage is changed to V_{RC1} = ±0.10 V or V_{RC2} = ±0.30 V depending on the load as shown in Figure 8-32 and Figure 8-33.

The Capacitive Mode Operation Detection Function operations as follows:

- **Period in Which the $Q_{(H)}$ is On**
  Figure 8-31 shows the RC pin waveform in the inductance area, and Figure 8-32 and Figure 8-33 shows the RC pin waveform in the capacitance area.
  In the inductance area, the RC pin voltage doesn't cross the plus side detection voltage in the downward direction during the on period of $Q_{(H)}$ as shown in Figure 8-31. On the contrary, in the capacitance area, the RC pin voltage crosses the plus side detection voltage in the downward direction. At this point, the capacitive mode operation is detected. Thus, $Q_{(H)}$ is turned off, and $Q_{(L)}$ is turned on, as shown in Figure 8-32 and Figure 8-33.

- **Period in Which the $Q_{(L)}$ is On**
  Contrary to the above of $Q_{(H)}$, in the capacitance area, the RC pin voltage crosses the minus side detection voltage in the upward directiont during the on period of $Q_{(L)}$ At this point, the capacitive mode operation is detected. Thus, $Q_{(L)}$ is turned off and $Q_{(H)}$ is turned on.

As above, since the capacitive mode operation is detected by pulse-by-pulse and the operating frequency is synchronized with the frequency of the capacitive mode operation, and the capacitive mode operation is prevented. In addition to the adjusting method of R_{OCP}, C3, and R6 in Section 8.17, R_{OCP}, C3, and R6 should be adjusted so that the absolute value of the RC pin voltage increases to more than $|V_{RC2}|$ = 0.30 V under the condition caused the capacitive mode operation easily, such as startup, turning off the mains input voltage, or output shorted. The RC pin voltage must be within the absolute maximum ratings of −6 to 6 V

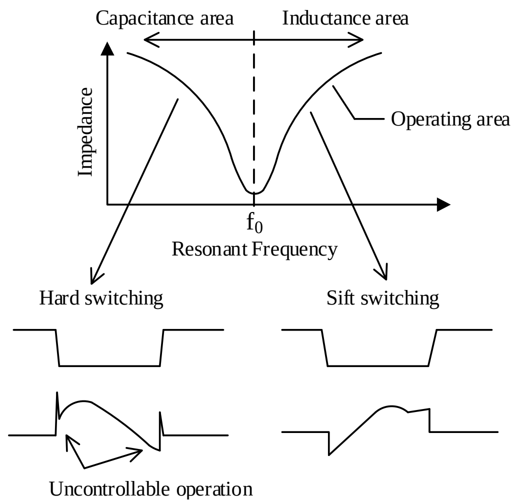

Figure 8-30. Operating Area of Resonant Power Supply

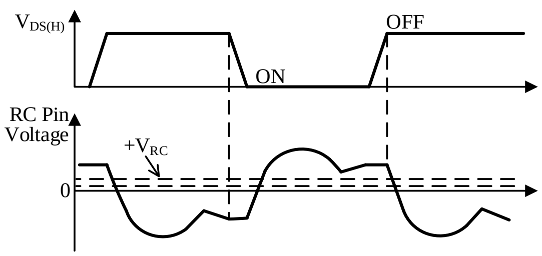

Figure 8-31. RC Pin Voltage in Inductance Area

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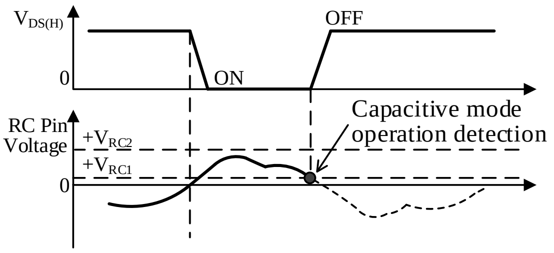

Figure 8-32. High-side Capacitive Mode Detection in Light Load

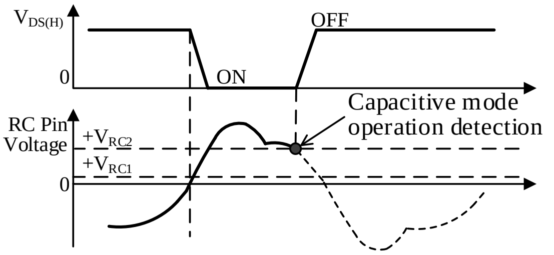

Figure 8-33. High-side Capacitive Mode Detection in Heavy Load

8.12 X-Capacitor Discharge Function

Generally, the line filter is set in the input circuit part of power supply as shown in Figure 8-34.

The voltage across the X-capacitor, C_X, must be decreased to 37 % of the peak voltage of AC input in one second to meet safety requirements such as IEC60950. Thus, the discharge resistor, R_{DIS}, is connected in parallel with C_X. While the AC input voltage is applied, R_{DIS} consumes power at all time. The dissipation power of R_{DIS}, P_{RDIS}, is calculated as follows:

$$P_{RDIS} = \frac{{V_{AC(RMS)}}^2}{R_{DIS}} \quad (8)$$

where, $V_{AC(RMS)}$ is the effective value of AC input voltage.

When the combined resistance of R_{DIS} is 1 MΩ and the AC input voltage is 265 V, P_{RDIS} becomes about 70 mW.

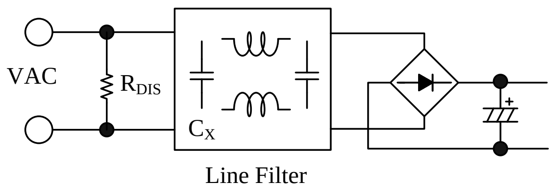

Figure 8-34. Typical Line Filter Circuit

In order to remove R_{ST} and improve the circuit efficiency, the IC has the X-capacitor Discharge Function. As shown in Figure 8-35, D_{ST1}, D_{ST2} and R_{ST} are connected to the ST pin from AC input line.

When AC voltage is input and VSEN pin voltage reaches to $V_{SEN(ON)}$ = 1.200 V at startup, the IC starts.

Then, following half-sinewaves are detected by two threshold voltages of the VSEN pin, $V_{SEN(OFF)1}$ = 1.000 V or $V_{SEN(AC)1}$ = 2.70 V (see Figure 8-36). Thus the IC's X-Capacitor Discharge Function achieves the wide range detection for universal specification.

When AC input voltage is cut off, the VSEN pin voltage becomes practically constant and the VSEN pin cannot detect the both threshold, $V_{SEN(OFF)1}$ and $V_{SEN(AC)1}$. Then, the CD pin capacitor, C_{CD}, is discharged by $I_{CD(SRC)}$ = –10.2 μA, and the CD pin voltage increases. When the CD pin voltage reaches to V_{CD1} = 3.0 V, the X-capacitor is discharged by the constant current, I_{ST} = 6.0 mA.

When the VSEN pin voltage becomes $V_{SEN(OFF)1}$ or $V_{SEN(AC)1}$, each internal threshold voltage becomes $V_{SEN(OFF)2}$ = 0.8 V or $V_{SEN(AC)2}$ = 2.4 V automatically. Thus, the input voltage can be detected stably.

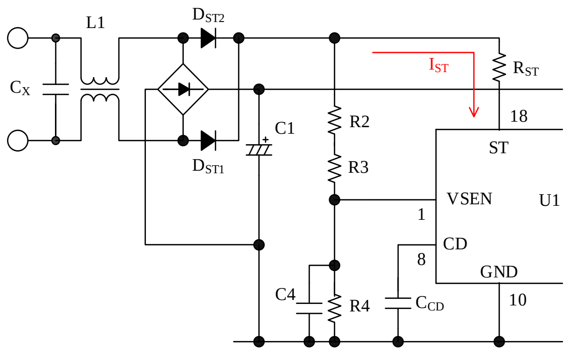

Figure 8-35. ST Pin Peripheral Circuit

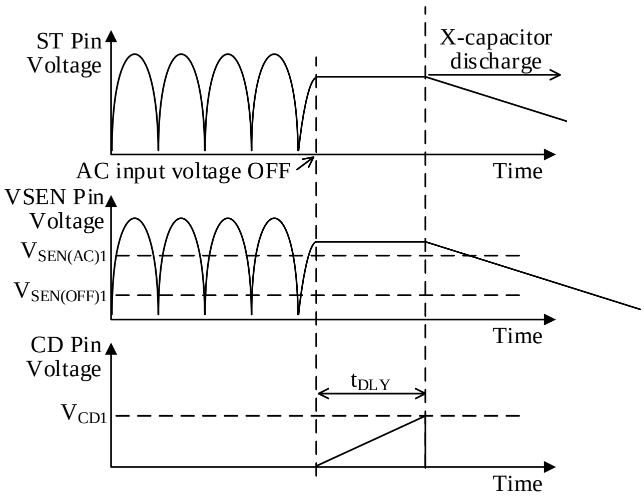

Figure 8-36. Operational Waveform of X-capacitor Discharge Function

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The time until the CD pin voltage reaches to V_{CD1} from the cutoff of AC input voltage is delay time, t_{DLY}.

The maximum value of t_{DLY}, t_{DLY_MAX}, can be set by the capacitor of CD pin and is calculated by Equation (10) in Section 8.16.2.

The recommend value of R_{ST} is 5.6 kΩ to 10 kΩ.
R_{ST} is applied high voltage and are high resistance, the following should be considered according to the requirement of the application:

- Select a resistor designed against electromigration, or
- Use a combination of resistors in series for that to reduce each applied voltage

8.13 Reset Detection Function

The magnetizing current means the circulating current applied for resonant operation, and that flows only into the primary-side circuit. During the startup period when the feedback control for the output voltage is inactive, if the magnetizing current cannot be reset in the on-period because of unbalanced operation, negative current may flows just before a power MOSFET turns off, and hard switching may occur, and stresses of power MOSFET may increase. To prevent this hard switching, the IC incorporates the Reset Detection Function.

Figure 8-38 shows the high-side operation and drain current waveform examples in normal resonant operation and reset failure operation. The Reset Detection Function extends the on-period until the absolute value of RC pin voltage, $|V_{RC1}|$, increases to 0.10 V or more. Thus, this function prevents the hard switching operation. When the on-period reaches the maximum reset time, $t_{RST(MAX)}$ = 5 µs, the on-period expires at that moment, and the power MOSFET turns off (see Figure 8-37).

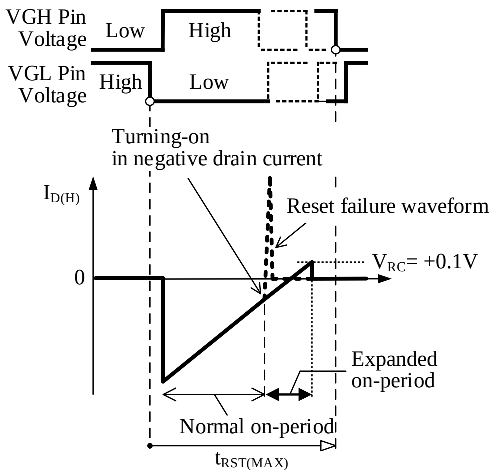

Figure 8-37. Reset Detection Operation Example

at High-side On-period

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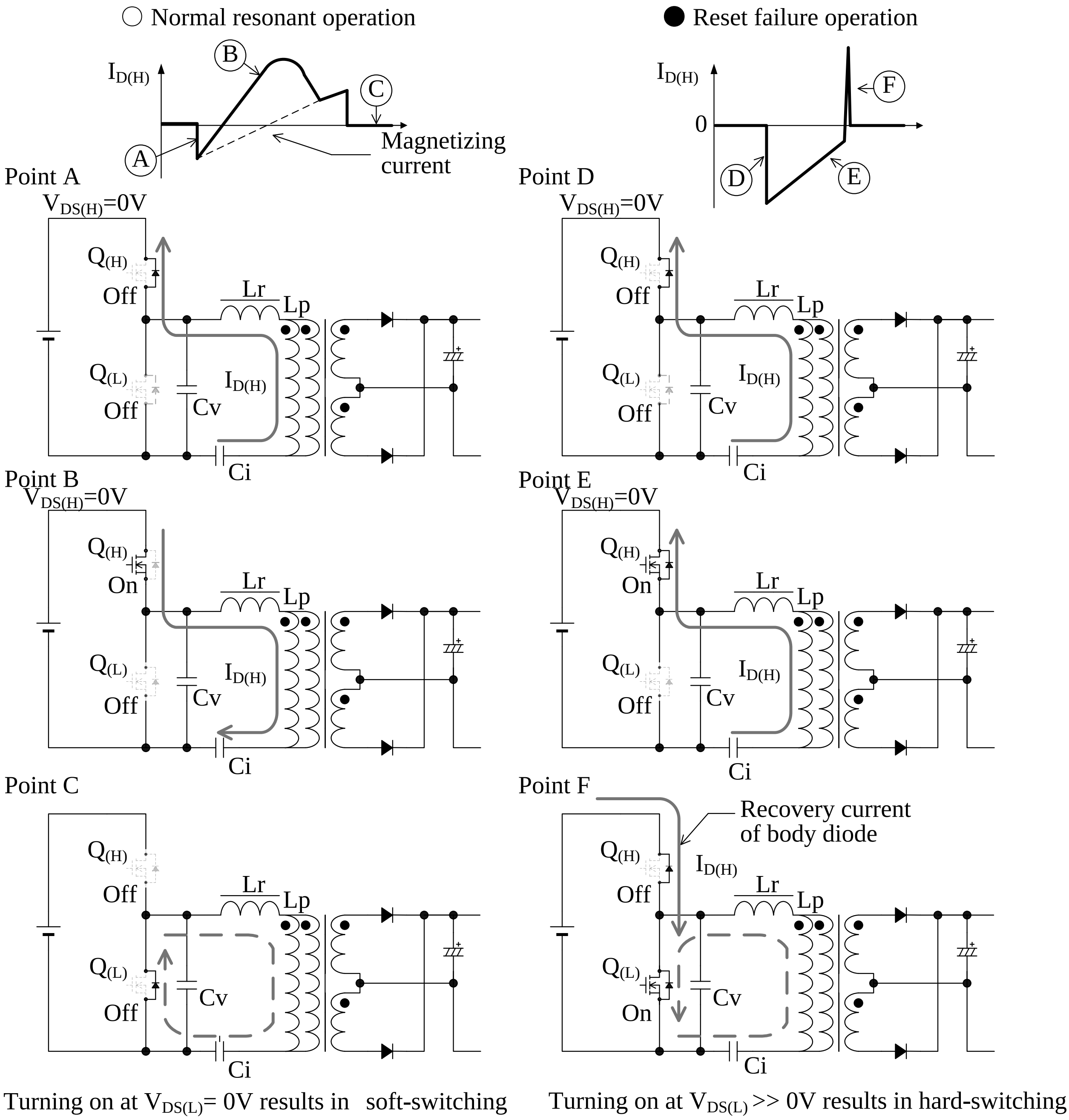

Figure 8-38. High-side Operation and Drain Current Waveform Examples in Normal Resonant Operation and in Reset Failure Operation

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8.14 Overvoltage Protection (OVP)

When the voltage between the VCC pin and the GND pin is applied to the OVP threshold voltage, $V_{CC(OVP)}$ = 32.0 V, or more, the Overvoltage Protection (OVP) is activated, and the IC stops switching operation in protection mode. When the OVP activates, the Bias Assist Function is disabled and VCC pin voltage decreases. Then the VCC pin voltage decreases to $V_{CC(P.OFF)}$ = 8.9 V, the Undervoltage Lockout (UVLO) Function is activated, and the IC reverts to the state before startup again.

After that, the startup circuit activates, and the VCC pin voltage increases to $V_{CC(ON)}$ = 17.0 V, and the IC starts operation. During the protection mode, restart and stop are repeated. When the fault condition is removed, the IC returns to normal operation automatically. When the auxiliary winding supplies the VCC pin voltage, the OVP is able to detect an excessive output voltage, such as when the detection circuit for output control is open in the secondary-side circuit because the VCC pin voltage is proportional to the output voltage.

The output voltage of the secondary-side circuit at OVP operation, $V_{OUT(OVP)}$, is approximately given as below:

$$V_{OUT(OVP)} = \frac{V_{OUT(NORMAL)}}{V_{CC(NORMAL)}} \times 32(V) \qquad (9)$$

where, $V_{OUT(NORMAL)}$ is output voltage in normal operation, and $V_{CC(NORMAL)}$ is VCC pin voltage in normal operation

8.15 REG Overvoltage Protection (REG_OVP)

The IC has REG Overvoltage Protection (REG_OVP) for the overvoltage of the REG pin.

When the REG pin voltage increases to REG Pin OVP Threshold Voltage, $V_{REG(OVP)}$ = 12.4 V, the REG_OVP is activated, and the IC stops switching operation and fixes the REG pin voltage to ground level.

When the REG_OVP activates, the Bias Assist Function is disabled and VCC pin voltage decreases. Then the VCC pin voltage decreases to $V_{CC(P.OFF)}$ = 8.9 V, the Undervoltage Lockout (UVLO) Function is activated, and the IC reverts to the state before startup again.

After that, the startup circuit activates, and the VCC pin voltage increases. When the VCC pin voltage reaches to $V_{CC(ON)}$ = 17.0 V, the IC starts operation and the VCC pin voltage decreases. When the VCC pin voltage decreases to $V_{CC(BIAS)}$, FB pin voltage increases and switching operation starts.

When the switching operation starts at RC pin voltage within V_{RC1} = ±0.10 V, C7 connected to CL pin is rapidly charged by $I_{CL(SRC)2}$ = −135 μA. When the CL pin voltage reaches to $V_{CL(OLP)}$ = 4.2 V, the IC stops switching operation and restarts after decreasing to $V_{CC(OFF)}$.

In this way, the intermittent operation by the CL pin protection and the UVLO is repeated.

When the fault condition is removed, the IC returns to normal operation automatically.

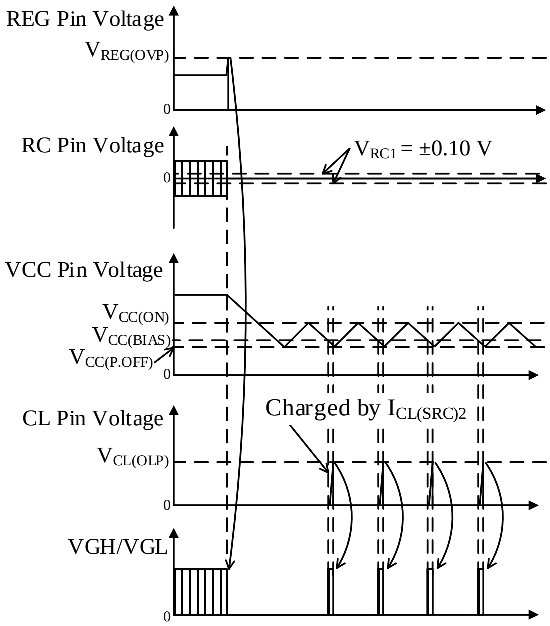

Figure 8-39. REG_OVP Waveform

8.16 AC Input Voltage Detection Function

This function has the following:

- AC Input Overvoltage Function (HVP)
- Brown-in and Brown-out Function

This function turns on and off switching operation according to the VSEN pin voltage detecting the AC input voltage, and thus prevents excessive input current and over heating. Section 8.16.1 shows HVP, Section 8.16.2 shows Brown-in and Brown-out Function. Figure 8-40 shows the pherepheral circuit of VSEN pin. Figure 8-41 shows AC Input Voltage Detection Function operational waveforms.

8.16.1 AC Input Overvoltage Function (HVP)

When the AC input voltage increases from steady state and the VSEN pin voltage reaches $V_{SEN(HVP)}$ = 5.6 V or more, AC Input Overvoltage Function (HVP) activates and the IC stops switching operation. During the HVP operation, the intermittent operation by UVLO is repeated (see Section 8.14). After that, when the AC input voltage decreases and the VSEN pin voltage falls to $V_{SEN(HVP)}$ or less, the IC starts switching operation.

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8.16.2 Brown-in and Brown-out Function

Even if the IC is in the operating state that the VCC pin voltage is $V_{CC(OFF)}$ or more, when the AC input voltage decreases from steady-state and the VSEN pin voltage falls to $V_{SEN(OFF)1}$ = 1.000 V or less for the delay time, t_{DLY}, the IC stops switching operation.

When the AC input voltage increases and the VSEN pin voltage reaches $V_{SEN(ON)}$ = 1.200 V or more in the operating state that the VCC pin voltage is $V_{CC(OFF)}$ or more, the IC starts switching operation.

The maximum delay time, t_{DLY_MAX}, can be calculated by Equation (10).

$$t_{DLY\_MAX} = \frac{V_{CD1} \times C_{CD}}{|I_{CD(SRC)}|} \qquad (10)$$

Where,

V_{CD1} is CD Pin Threshold Voltage 1 (3.0 V),

C_{CD} is the capacitance value of CD pin connected capacitor (about 0.1µF to 0.47µF), and

$I_{CD(SRC)}$ is CD Pin Source Current (–10.2 µA)

For example, if C_{CD} is 0.1µF,

$$t_{DLY\_MAX} = \frac{3.0\ \mathrm{V} \times 0.1\mu\mathrm{F}}{|-10.2\ \mu\mathrm{A}|} \approx 29.4\ \mathrm{ms}$$

Neglecting the effect of both input resistance and forward voltage of rectifier diode, the effective value of AC input voltage when HVP and Brown-in and Brown-out function is activated is calculated as follows:

$$V_{AC(OP)} = \frac{1}{\sqrt{2}} \times V_{SEN(TH)} \times \left(1 + \frac{R2 + R3}{R4}\right) \qquad (11)$$

where,

$V_{DC(OP)}$ is the effective value of AC input voltage when HVP and Brown-in and Brown-out function is activated, and

$V_{SEN(TH)}$ is any one of threshold voltage of VSEN pin (see Table 8-1).

Table 8-1. VSEN Pin Threshold Voltage

Parameter	Symbol	Value (Typ.)
VSEN Pin HVP Threshold Voltage	$V_{SEN(HVP)}$	5.6 V
VSEN Pin Threshold Voltage (On)	$V_{SEN(OFF)1}$	1.000 V
VSEN Pin Threshold Voltage (Off)	$V_{SEN(ON)}$	1.200 V

Because R2 and R3 are applied high voltage and are high resistance, the following should be considered:

- Select a resistor designed against electromigration according to the requirement of the application, or
- Use a combination of resistors in series for that to reduce each applied voltage.

The reference value of R2 is about 10 MΩ.

C4 shown in Figure 8-40 is for reducing noises. The value is 1000 pF or more, and the reference value is about 0.01 µF.

The value of R2, R3 and R4 and C4 should be selected based on actual operation in the application.

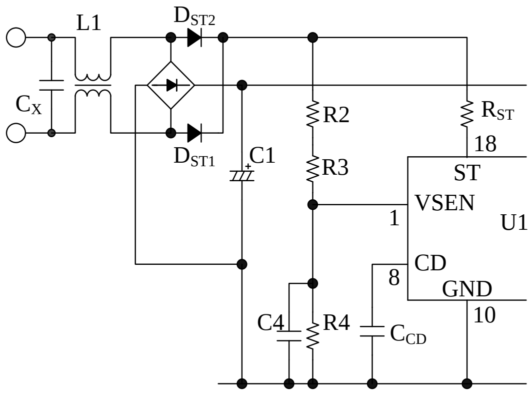

Figure 8-40. VSEN Pin Pherepheral Circuit

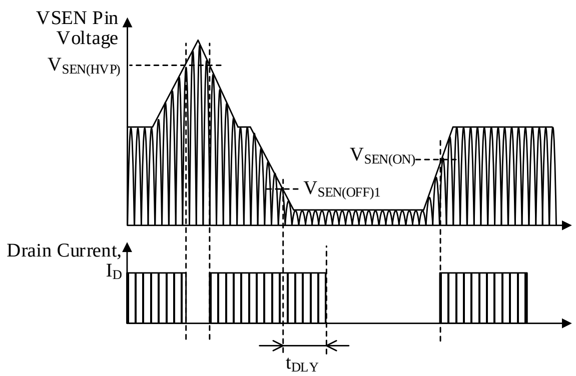

Figure 8-41. AC Input Voltage Detection Function Operational Waveforms

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8.17 Overcurrent Protection (OCP)

The Overcurrent Protection (OCP) detects the drain current, I_D, on pulse-by-pulse basis, and limits output power. In Figure 8-42, this circuit enables the value of C3 for shunt capacitor to be smaller than the value of Ci for current resonant capacitor, and the detection current through C3 is small. Thus, the loss of the detection resistor, R_{OCP}, is reduced, and R_{OCP} is a small-sized one available.

There is no convenient method to calculate the accurate resonant current value according to the mains input and output conditions, and others. Thus, R_{OCP}, C3, and C6 should be adjusted based on actual operation in the application. The following is a reference adjusting method of R_{OCP}, C3, R6, and C8:

- C3 and R_{OCP}
  C3 is 100pF to 330pF (around 1 % of Ci value).
  R_{OCP} is around 100 Ω.
  Given the current of the high side power MOSFET at ON state as $I_{D(H)}$. R_{OCP} is calculated Equation (12).
  The detection voltage of R_{OCP} is used the detection of the capacitive mode operation (see Section 8.11). Therefore, setting of R_{OCP} and C3 should be taken account of both OCP and the capacitive mode operation.

$$R_{OCP} \approx \frac{V_{OC(L)}}{I_{D(H)}} \times \left(\frac{C3 + Ci}{C3}\right) \quad (12)$$

- R6 and C8 are for high frequency noise reduction.
  R6 is 100 Ω to 470 Ω. C6 is 100 pF to 1000 pF.

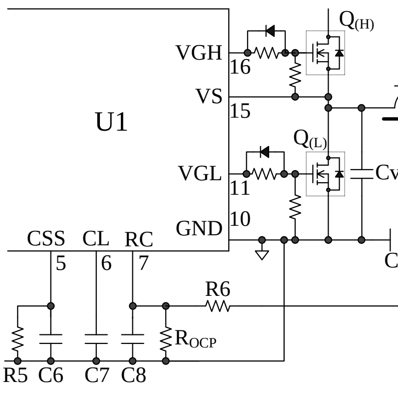

Figure 8-42. RC Pin Peripheral Circuit

The OCP operation has two-step threshold voltage as follows:

Step I, RC Pin Threshold Voltage (Low), $V_{RC(L)}$:

This step is active first. When the absolute value of the RC pin voltage increases to more than $|V_{OC(L)}| = 1.9$ V, C6 connected to the CSS pin is discharged by $I_{CSS(L)} = 1.8$ mA. Thus, the switching frequency increases, and the output power is limited. During discharging C6, when the absolute value of the RC pin voltage decreases to $|V_{RC(L)}|$ or less, the discharge stops.

Step II, RC Pin Threshold Voltage (High-speed), $V_{RC(S)}$:

This step is active second. When the absolute value of the RC pin voltage increases to more than $|V_{RC(S)}| = 2.80$ V, the high-speed OCP is activated, and power MOSFETs reverse on and off. At the same time, C6 is discharged by $I_{CSS(S)} = 20.5$ mA. Thus, the switching frequency quickly increases, and the output power is quickly limited. This step operates as protections for exceeding overcurrent, such as the output shorted.

When the absolute value of the RC pin voltage decreases to $|V_{RC(S)}|$ or less, the operation is changed to the above Step I.

8.18 Overload Protection (OLP)

Figure 8-43 shows the Overload Protection (OLP) waveforms.

When the absolute value of RC pin voltage increases to $|V_{RC(L)}| = 1.9$ V by increasing of output power, the Overcurrent Protection (OCP) is activated. After that, the C7 connected to CL pin is charged by $I_{CL(SRC)1} = -17$ μA. When the OCP state continues and CL pin voltage increases to $V_{CL(OLP)}$, the OLP is activated.

When CL pin voltage becomes the threshold voltage of OLP, $V_{CL(OLP)} = 4.2$ V, the OLP is activated and the switching operation stops. During the OLP operation, the intermittent operation by UVLO is repeated (see Section 8.14). When the fault condition is removed, the IC returns to normal operation automatically.

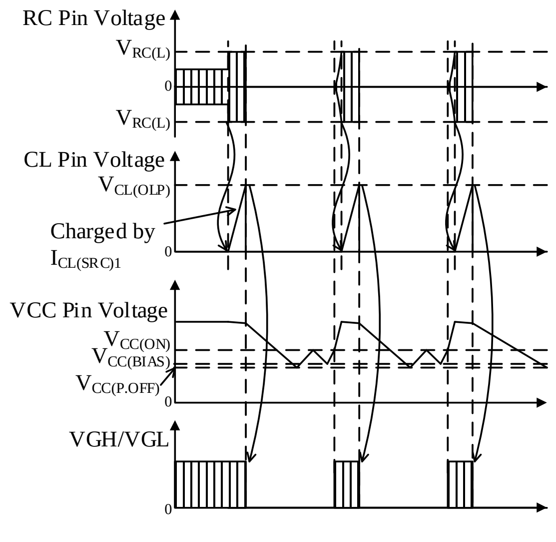

Figure 8-43. OLP Waveform

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8.19 Thermal Shutdown (TSD)

When the junction temperature of the IC reach to the Thermal Shutdown Temperature $T_{j(TSD)}$ = 140 °C (min.), Thermal Shutdown (TSD) is activated and the IC stops switching operation. When the VCC pin voltage is decreased to $V_{CC(P.OFF)}$ = 8.9 V or less and the junction temperature of the IC is decreased to less than $T_{j(TSD)}$, the IC restarts.

During the protection mode, restart and stop are repeated. When the fault condition is removed, the IC returns to normal operation automatically.

9. Design Notes

9.1 External Components

Take care to use the proper rating and proper type of components.

9.1.1 Input and output electrolytic capacitors

Apply proper derating to ripple current, voltage, and temperature rise. The electrolytic capacitor of high ripple current and low impedance types, designed for switch mode power supplies, is recommended to use.

9.1.2 Resonant transformer

The resonant power supply uses the leakage inductance of transformer. Therefore, in order to reduce the effect of the eddy current and the skin effect, the wire of transformer should be used a bundle of fine litz wires.

9.1.3 Current detection resistor, R_{OCP}

Choose a type of low internal inductance because a high frequency switching current flows to R_{OCP}, and of properly allowable dissipation.

9.1.4 Current resonant capacitor, Ci

Large resonant current flows through Ci. Ci should use the polypropylene film capacitor with low loss and high current capability. In addition, Ci must be considered its frequency characteristic since high frequency current flows.

9.1.5 Gate Pin Peripheral Circuit

The VGH pin and the VGL pin are gate drive output pins for external power MOSFETs.

The peak source current of both of them is –540 mA, and the peak sink current is 1.50 A.

D_S of Figure 9-1 makes a turn-off speed faster.

R_A and Ds should be adjusted considering power losses of power MOSFETs, gate waveforms (reduction of ringing caused by pattern layout and others), and EMI noise.

R_{GS} prevents malfunctions caused by steep dv/dt at turning off power MOSFET. R_{GS} is recommended to be a resistor of 10 k to 100 kΩ close to the Gate and the Source of power MOSFET.

When the gate resistances are adjusted, the gate waveforms should be checked that the dead time is ensured as shown in Figure 9-2.

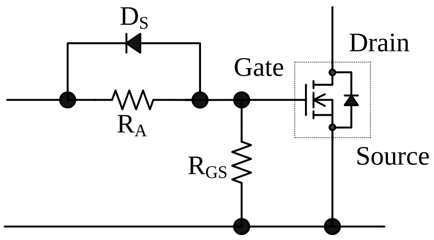

Figure 9-1. Power MOSFET Peripheral Circuit

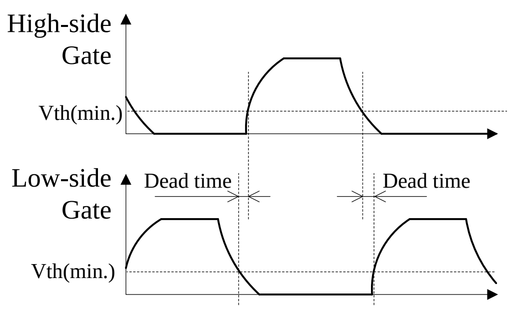

Figure 9-2. Dead Time Confirmation

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9.2 PCB Trace Layout and Component Placement

Since the PCB circuit design and the component layout significantly affect the power supply operation, EMI noise, and power dissipation, the high frequency trace of PCB shown in Figure 9-3 should be designed low impedance by small loop and wide trace.

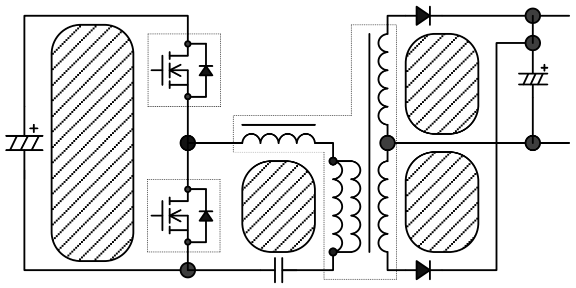

Figure 9-3 High Frequency Current Loops (Hatched Areas)

In addition, the PCB circuit design should be taken account as follows:

Figure 9-4 shows the circuit design example.

1) Main Circuit Trace Layout
This is the main trace containing switching currents, and thus it should be as wide trace and small loop as possible.

2) Control Ground Trace Layout
When large current flows into the control ground trace, the operation of IC might be affected by it. The control ground trace should be separate from the main circuit trace, and should be connected at a single point grounding as close to the GND pin as possible.

3) VCC Trace Layout
This is the trace for supplying power to the IC, and thus it should be as small loop as possible. If C3 and the IC are distant from each other, placing a film capacitor C_f (about 0.1 µF to 1.0 µF) close to the VCC pin and the GND pin is recommended.

4) Peripheral Components for the IC Control
These components should be placed close to the IC, and be connected to the IC pin as short as possible.

5) Bootstrap Circuit Components
These components should be connected to the IC pin as short as possible, and the loop for these should be as small as possible.

6) Secondary Side Rectifier Smoothing Circuit Trace Layout
This is the trace of the rectifier smoothing loop, carrying the switching current, and thus it should be as wide trace and small loop as possible.

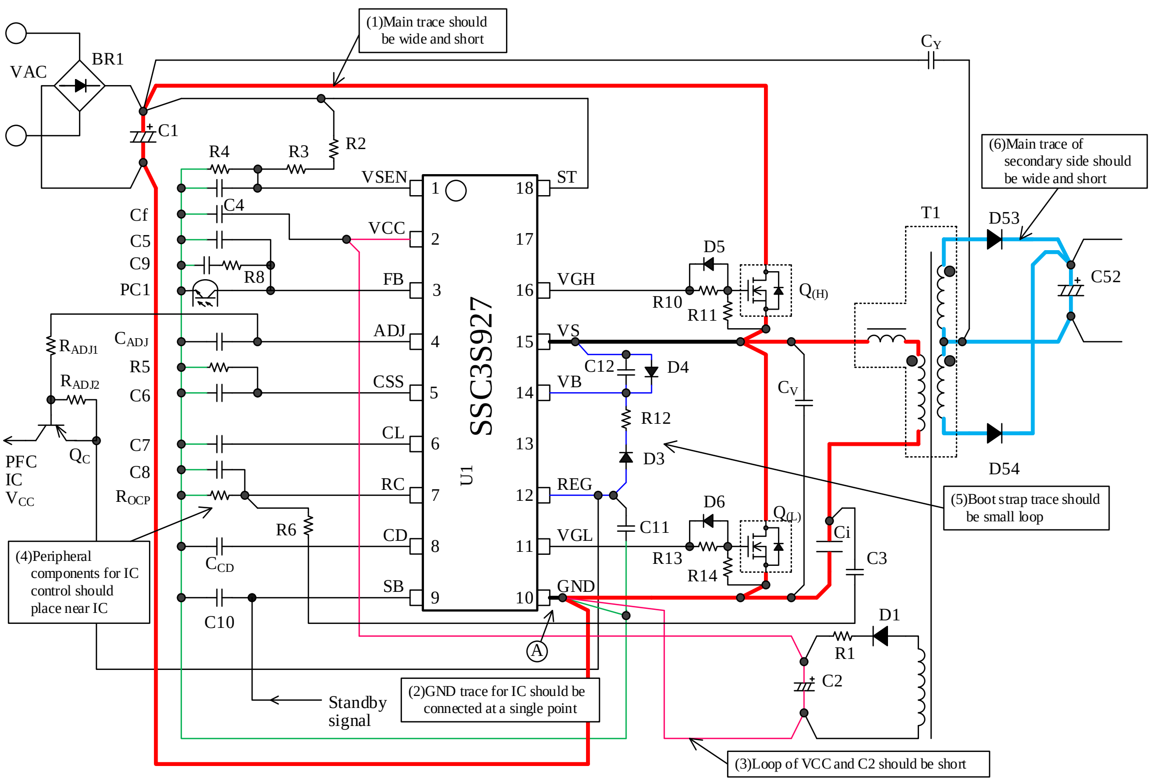

Figure 9-4 Peripheral Circuit Trace Example Around the IC

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10. Pattern Layout Example

The following show the PCB pattern layout example and the schematic of circuit using SSC3S927.

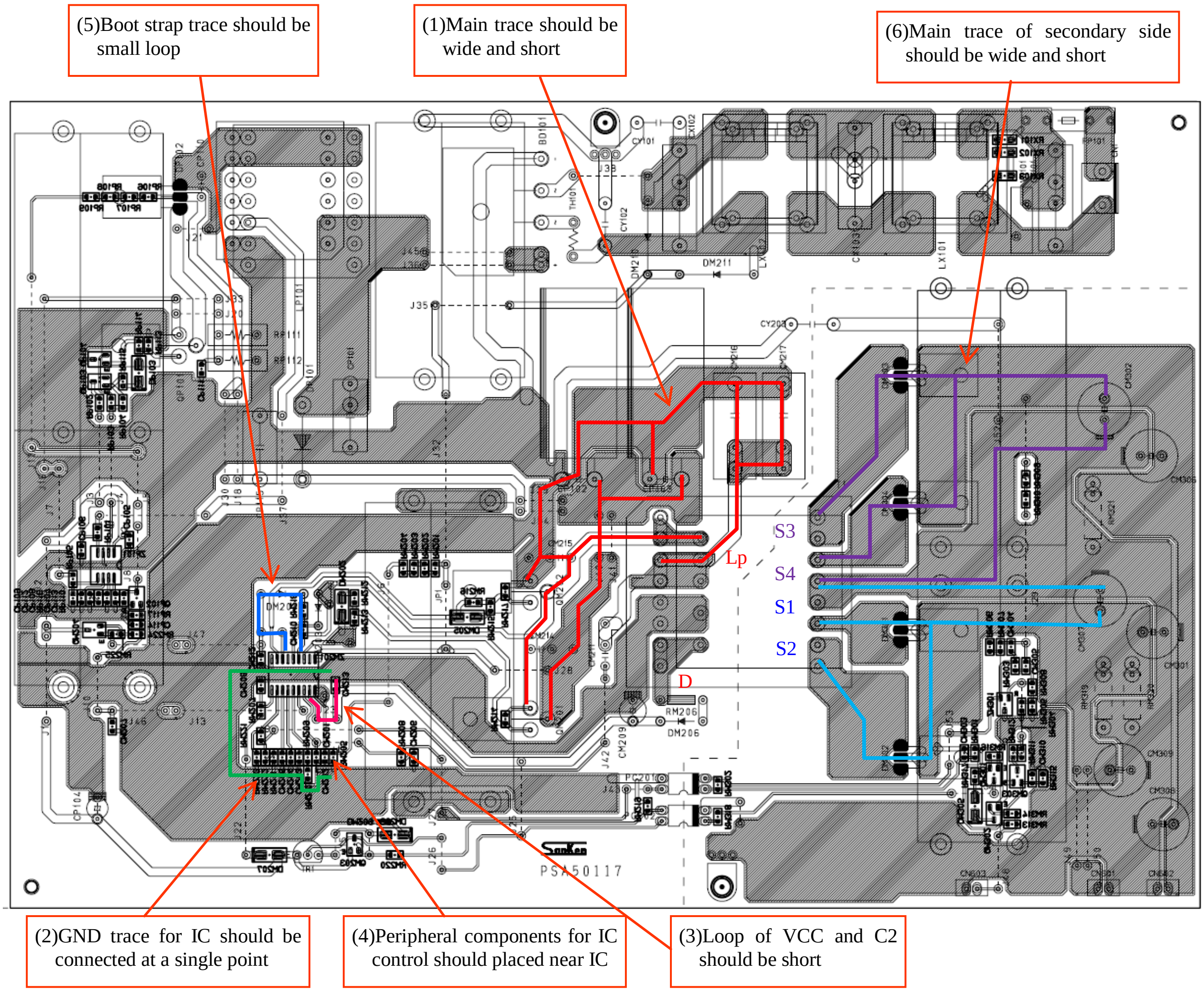

Figure 10-1. PCB Pattern Layout Example

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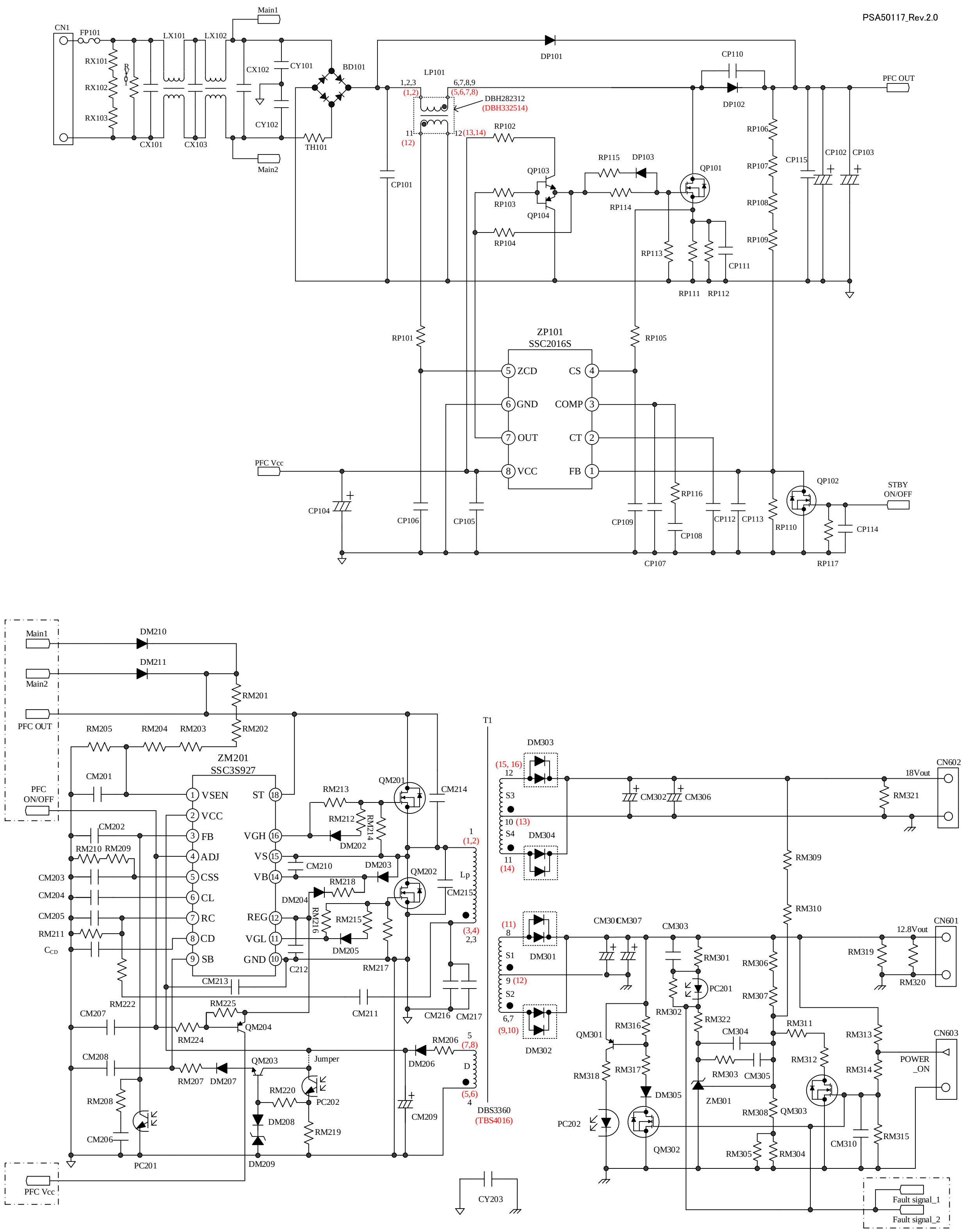

Figure 10-2. PCB Pattern Layout Example Circuit

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